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Universal Continuous-Time Filter Challenges Discrete Designs

by Max Hauser

The LTC1562 is the first in a new family of tunable, DC-accurate, continuous-time filter products featuring very low noise and distortion. It contains four independent 2nd order, 3-terminal filter blocks that are resistor programmable for lowpass or bandpass filtering functions up to 150kHz, and has a complete PC board footprint smaller than a dime. Moreover, the part can deliver arbitrary continuous-time pole-zero responses, including highpass, notch and elliptic, if one or more programming resistors are replaced with capacitors. The center frequency (f_0) of the LTC1562 is internally trimmed, with an absolute accuracy of 0.5%, and can be adjusted independently in each 2nd order section from 10kHz to 150kHz by an external resistor. Other features include:

- ❑ Rail-to-rail inputs and outputs
- ❑ Wideband signal-to-noise ratio (SNR) of 103dB
- ❑ Total harmonic distortion (THD) of –96dB at 20kHz, –80dB at 100kHz
- ❑ Built-in multiple-input summing and gain features; capable of 118dB dynamic range
- ❑ Single- or dual-supply operation, 4.75V to 10.5V total
- ❑ "Zero-power" shutdown mode under logic control
- ❑ No clocks, PLLs, DSP or tuning cycles required

The LTC1562, in the SSOP package, provides eight poles of programmable continuous-time filtering in a total surface mount board area (including the programming resistors) of 0.24 square inches (155 mm^2)—smaller than a U.S. 10-cent coin. This filter can also replace op amp–R-C active filter circuits and LC filters in applications requiring compactness, flexibility, high dynamic range or fewer precision components.

What's Inside?

As shown in Figure 1, the LTC1562 includes four identical 3-terminal blocks. Each contains active circuitry, precision capacitors and precision resistors, forming a flexible 2nd order filter core. These blocks are designed to make filters as easy to configure as op amps. The 3-terminal arrangement minimizes the number of external parts necessary for a complete 2nd order filter with arbitrarily programmable f_0, Q and gain. Figure 2 shows the contents of one block, along with three external resistors, forming a complete lowpass/bandpass filter (the most basic application of the LTC1562). In Figure 2, a lowpass response appears between the V_{IN} source and the LP output pin, and simultaneously a bandpass response is available at the BP output pin. Both outputs have rail-to-rail capability for the maximum possible signal swing, and hence, maximum signal-to-noise ratio (SNR).

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Issue Highlights

Our cover article for this issue introduces a new filter product, the LTC1562. The LTC1562 is the first in a new family of tunable, DC-accurate, continuous-time filter products featuring very low noise and distortion. It contains four independent 2nd order, 3-terminal filter blocks that are resistor programmable for lowpass or bandpass filtering functions up to 150kHz, and has a complete PC board footprint smaller than a dime.

Data converters are strongly represented in this issue, with a new DAC and several new ADCs:

The LTC1427-50 is a 10-bit, current-source-output DAC with an SMBus interface. This device provides precision, full-scale current of 50µA ±1.5% at room temperature (±3% over temperature), wide output voltage DC compliance (from –15V to [V_{CC} – 1.3V]) and guaranteed monotonicity over a wide supply-voltage range. It is an ideal part for applications in contrast/brightness control or voltage adjustment in feedback loops.

We also introduce the LTC1604, a fast, high performance 16-bit sampling ADC in a tiny 36-pin SSOP package. This device runs at 333ksps and delivers excellent DC and AC performance. It operates on ±5V supplies and typically draws only 220mW. It is a complete differential, high speed, low power, 16-bit sampling ADC that requires no external components. The LTC1604 also provides two power-shutdown modes, NAP and SLEEP, to reduce power consumption during inactive periods. It not only offers the performance of the best hybrids but also provides low power, small size, an easy-to-use interface and the low cost of a monolithic part.

A new, versatile 14-bit ADC, the LTC1418, can digitize at 200ksps while consuming only 15mW from a single 5V supply. The LTC1418 is designed to be easy to use and adaptable, requiring little or no support circuitry in a wide variety of applications. It features 0.25LSB INL max and 1LSB DNL max, parallel and serial data output modes and NAP and SLEEP power-shutdown modes.

In the power conversion arena, we debut two new micropower DC/DC converters designed to provide power from a single-cell or higher input voltage, the LT1308 and the LT1317. The LT1308 is intended for generating power on the order of 2W–5W, for RF power amplifiers in GSM or DECT terminals or for digital-camera power supplies. The LT1317, intended for lower power requirements, operates from an input voltage as low as 1.5V. It can generate 100mW to 2W of power. Both devices feature Burst Mode™ operation for high efficiency at light loads. Both devices switch at 600kHz; this high frequency keeps associated power components small and flat.

On the interface front, we present a new multiprotocol chip set that is guaranteed to be Net1 and Net2 compliant. The LTC1543/LTC1544/LTC1344A chip set creates a complete software-selectable serial interface using an inexpensive DB-25 connector. The LTC1543 is a dedicated data/clock chip and the LTC1544 is a control-signal chip. The chip set supports the V.28 (RS232), V.35, V.36, RS449, EIA-530, EIA-530A and X.21 protocols in either DTE or DCE mode.

In the Design Ideas section, we feature a 1kHz, 8th order Butterworth highpass filter, power gain stages to extend the output-power capability of the LT1533 ultralow noise switching regulator, a nanopower zero-bias detector and a complete battery backup solution based on a single NiCd cell and the LT1558 battery-backup controller.

We conclude with Design Information on the LTC1660 10-bit octal DAC and the LTC1632 SMBus switch controller and a pair of New Device Cameos.

LTC in the News...

LTC Reports Another Strong Quarter

"Demand for our products remained strong and well diversified across end markets," said Robert Swanson, president and CEO of Linear Technology Corporation. "We had another strong quarter, achieving record levels for sales and profits. The turmoil in the Asian financial markets did not have a material impact on our business in this quarter, although we continue to closely monitor this geographical area for its impact in the future."

Douglas Lee, an analyst at NationsBanc Montgomery Securities in San Francisco, predicts that Linear Technology will "see a sequential sales growth of about 7% for the March quarter." This was reported in the January 19, 1998 issue of *Electronic Buyers' News*.

Net sales for the second quarter ended December 28, 1997 were $117,004,000, an increase of 30% over net sales of $90,080,000 for the second quarter of the previous year. The Company also reported net income for the quarter of $43,582,000, an increase of 38% over the $31,631,000 reported for the second quarter of last year.

Diluted earnings per share (EPS) were $0.55 compared to $0.40 for the similar quarter last year. This is the first quarter that earnings per share (EPS) are reported in compliance with the new Financial Accounting Standards Board pronouncement No. 128. Diluted EPS is analogous to the methodology the Company used in the past in reporting EPS.

During the quarter, Linear Technology purchased 1,002,500 shares of its stock for $56.4 million, $5.9 million of which was paid after quarter end. A cash dividend of $0.40 will be paid on February 11, 1998 to shareholders of record on January 23, 1998

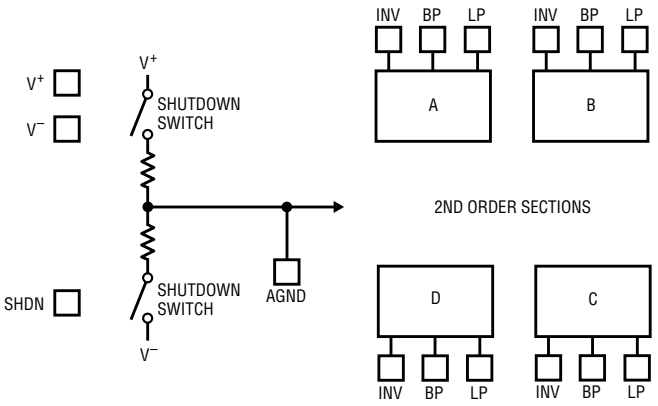

Figure 1. LTC1562 block diagram

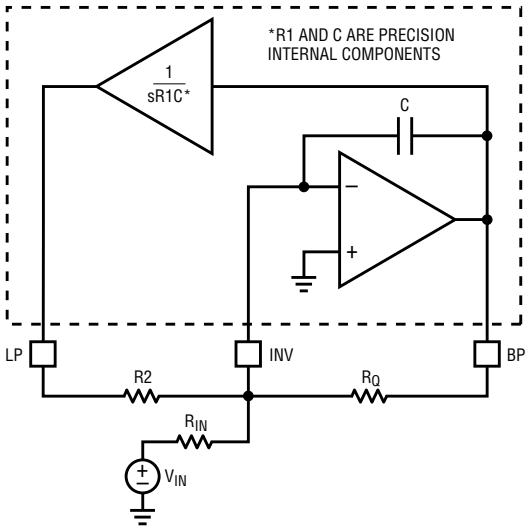

Figure 2. Single 2nd order section, illustrating connection with external resistors R2, R_{IN} and R_Q

LTC1562, continued from page 1

The LTC1562 is versatile; it is not limited to the lowpass/bandpass filter of Figure 2. Cascading multiple sections, of course, yields higher-order filters (Figure 3a). A highpass response results if the external input resistor (R_{IN} of Figure 2) is replaced by a capacitor, C_{IN}, which sets only gain, not critical frequencies (Figure 3b). Responses with arbitrary zeroes (for example, elliptic or notch responses) are implemented with feedforward connections with multiple 2nd order blocks, as shown in the application circuit in Figure 8. Moreover, the virtual-ground INV input gives each 2nd-order section the built-in capability for analog operations such as gain (preamplification), summing and weighting of multiple inputs, or accepting current or charge signals directly. These flexible 3-terminal elements are Operational Filter™ blocks.

Although the LTC1562 is offered in a 20-pin SSOP package, the LTC1562 is a 16-pin circuit; the extra pins are connected to the die substrate and should be returned to the negative power supply. In single-supply applications, these extra V– pins should be connected directly to a PC board's ground plane for the best grounding and shielding of the filter. 16-pin plastic DIP packaging is also available (consult the factory).

DC Performance and Power Shutdown

The LTC1562 operates from single or dual supply voltages, nominally 5V to 10V total. It generates an internal half-supply reference point (the AGND pin), establishing a reference voltage for the inputs and outputs in single-supply applications. In these applications, the AGND pin should be bypassed with a capacitor to the ground plane (at V–); the pin can be connected directly to ground when a split supply is used. The DC offset voltage from the filter input to the LP output for a typical 2nd order section (unity DC gain) is typically 5mV. Both outputs swing to within approximately 100mV of each supply rail with loads of 5kΩ and 30pF.

To save power in a "sleep" situation, a logic high input on the SHDN pin will put the LTC1562 into its shutdown mode, in which the chip's power supply current is reduced to only junction leakage (typically 2µA from a single 5V supply). The shutdown pin is designed to accept CMOS levels with 5V swing, for example, 0V and 5V logic levels when the LTC1562 is powered from either a single 5V or a split ±5V supply. Note that in the LTC1562, unlike some other products, a small bias current source (approximately 2µA) at the SHDN pin causes the chip to default to the shutdown state if this pin is left open. Therefore, the user must remember to connect the SHDN pin to a logic low for normal operation if the shutdown feature is not used. (This default-to-shutdown convention saves system power in the shutdown state, since it eliminates even the microampere current that would otherwise flow from the driving logic to the bias-current source.)

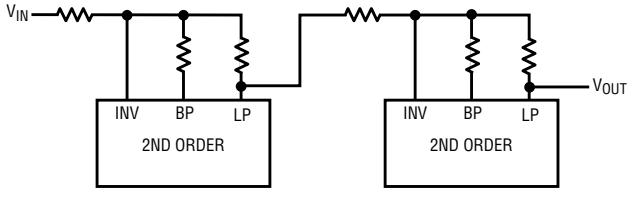

Figure 3a. Two 2nd order sections cascaded for higher order response

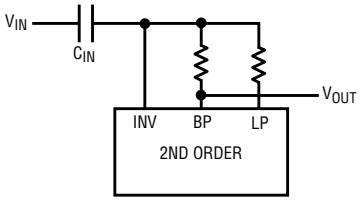

Figure 3b. 2nd order section configured for highpass output

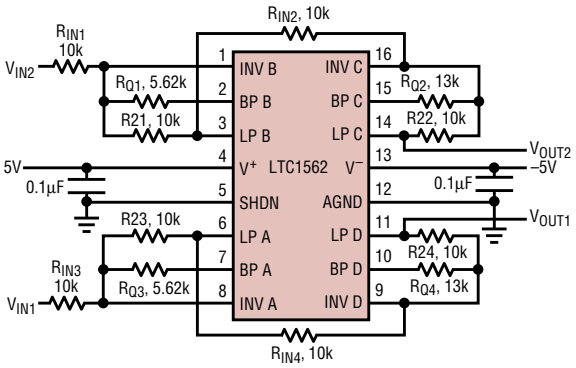

Figure 4. Dual, matched 4th order 100kHz Butterworth lowpass filter

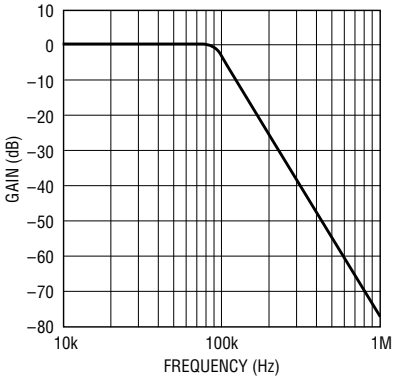

Figure 5. Frequency response of Figure 4's circuit

Frequency Responses

Lowpass filters with standard all-pole responses (Butterworth, Chebyshev, Bessel, Gaussian and so on) of up to 8th order (eight poles) can be realized with LTC1562 sections connected as in Figures 2 and 3a; practical examples appear later in this article. Resistor ratios program the standard filter parameters f_0, Q and gain; required values of these filter parameters can be found from tables or from software such as FilterCAD™ for Windows®, available free from LTC.

The "LP" and "BP" outputs of each 2nd order section, although named after their functions in Figure 2, can display other responses than lowpass and bandpass, respectively, if the external components are not all resistors. The highpass configuration of Figure 3b has a passband gain set by the ratio C_{IN}/C, where C is an internal 160pF capacitor in the LTC1562. The two resistors in Figure 3b control f_0 and Q, as in the other modes.

The LTC1562 is the first truly compact universal active filter, yet it offers instrumentation-grade performance rivaling much larger discrete-component designs.

Bandpass applications can use the LTC1562 in either of two ways. In the basic configuration, with the only external components being resistors (Figure 2), the BP output has a bandpass response from V_{IN}. With an input capacitor, as in Figure 3b, the BP output has a highpass response as noted above and the LP pin shows a bandpass response.

The f_0 range is approximately 10kHz–150kHz, limited mainly by the magnitudes of the external resistors required. At high f_0 these resistors fall below 5k, heavily loading the outputs of the LTC1562 and leading to increased THD and other effects. A lower f_0 limit of 10kHz reflects an arbitrary resistor magnitude limit of 1 Megohm. The LTC1562's MOS input circuitry can accommodate higher resistor values than this, but junction leakage current from the input-protection circuitry may cause DC errors.

Design formulas and further details on frequency-response programming appear in the LTC1562 data sheet.

Low Noise and Distortion

The active (that is, amplifier) circuitry in the LTC1562 was designed expressly for filtering. Because of this, filter noise is due primarily to the circuit resistors rather than to the amplifiers. The amplifiers also exhibit exceptional linearity, even at high frequencies (patents pending). The noise and distortion performance for filters built with the LTC1562 compares favorably with filters using expensive, high performance, off-the-shelf op amps that demand many more external parts and far more board area (we know, because we've

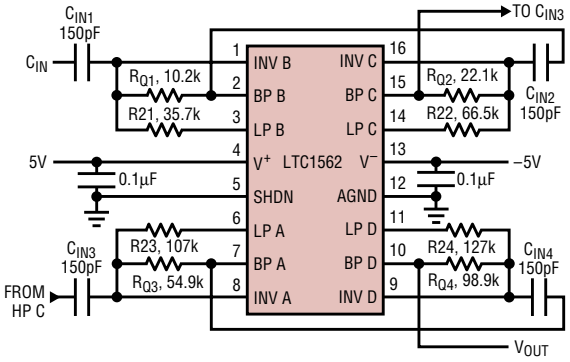

Figure 6. 8th order Chebyshev highpass filter with 0.05dB ripple (f_{CUTOFF} = 30kHz)

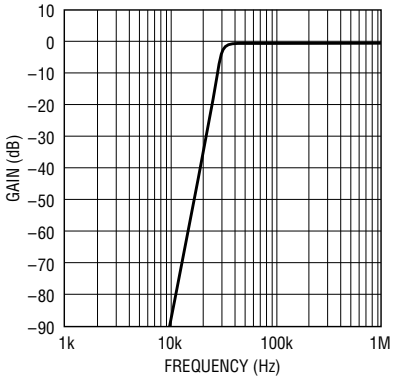

Figure 7. Frequency response of Figure 6's circuit

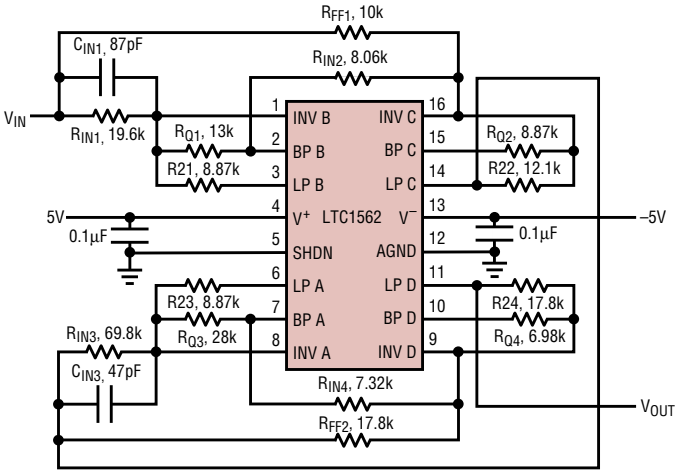

Figure 8. 8th order 100kHz elliptic lowpass filter

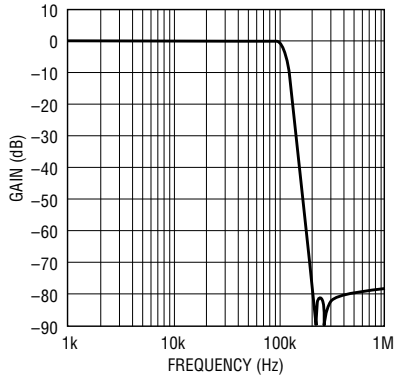

Figure 9. Frequency response of Figure 8's circuit.

built them). The details of this performance depend on Q and other parameters and are reported for specific application examples below. As with other low distortion circuits, accurately measuring distortion performance requires both an input signal and distortion-analyzing equipment with adequately low distortion floors.

Low level signals can exploit a low noise preamplification feature in the LTC1562. A 2nd order section operated with unity gain, Q = 1 and f_0 = 100kHz shows a typical output noise of 24µV_{RMS}, which gives a 103dB SNR with full-scale output from a 10V total supply. However, reducing the value of R_{IN} in Figure 2 increases the gain without a proportional increase in the output noise (unlike many active filters). A gain of 100 (40dB) with the same Q and f_0 gives a measured output noise of 449µV_{RMS} or an input-referred noise of 4.5µV_{RMS}—a 78dB output SNR with an input that is 40dB down. Thus, the same circuit can handle a wide range of input levels with high SNR by changing (or switching) the input resistor. In the example just cited, the ratio of maximum input signal to minimum input noise, by changing R_{IN}, is 118dB.

Dual 4th Order 100kHz Butterworth Lowpass Filter

The practical circuit in Figure 4 is a dual lowpass filter with a Butterworth (maximally-flat-passband) frequency response. Each half gives a DC-accurate, unity-passband-gain lowpass response with rail-to-rail input and output. With a 10V total power supply, the measured output noise for one filter is 36µV_{RMS} in a 200kHz bandwidth, and the large-signal output SNR is 100dB. Measured THD at 1V_{RMS} input is –83.5dB at 50kHz and –80dB at 100kHz. Figure 5 shows the frequency response of one filter.

8th Order 30kHz Chebyshev Highpass Filter

Figure 6 shows a straightforward use of the highpass configuration in Figure 3b with some practical values. Each of the four cascaded 2nd order sections has an external capacitor in the input path, as in Figure 3b. The resistors in Figure 6 set the f_0 and Q values of the four sections to realize a Chebyshev (equiripple-passband) response with 0.05dB ripple and a 30kHz highpass corner. Figure 7 shows the frequency response. Total output noise for this circuit is 40µV_{RMS}.

8th Order 100kHz Elliptic Lowpass Filter

Figure 8 illustrates how sharp-cutoff filtering can exploit the Operational Filter capabilities of the LTC1562. In this design, two external capacitors are added and the virtual-ground inputs of the LTC1562 sum parallel paths to obtain two notches in the stopband of a lowpass filter, as plotted in Figure 9. This response falls 80dB in one octave; the total output noise is 46µV_{RMS} and the Signal/

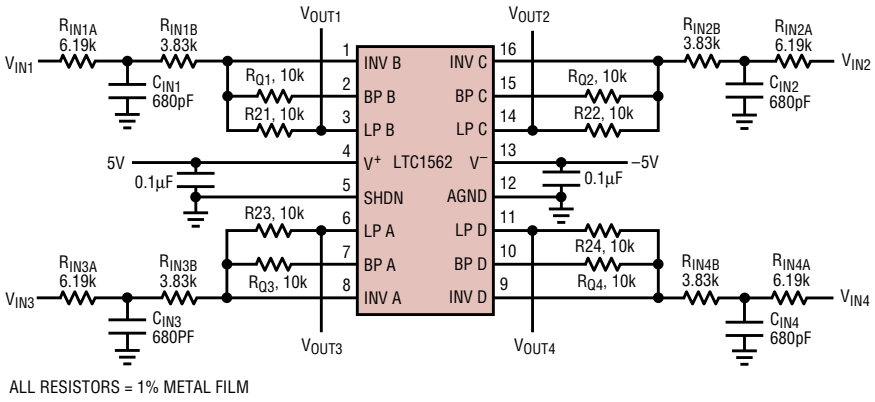

Figure 10. Quad 3-pole 100kHz Butterworth lowpass filter

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An SMBus-Controlled 10-Bit, Current Output, 50µA Full-Scale DAC

by Ricky Chow

The LTC1427-50 is a 10-bit, current-output DAC with an SMBus interface. This device provides precision, full-scale current of 50µA ±1.5% at room temperature (±2.5% over temperature), wide output voltage DC compliance (from –15V to (V_{CC} – 1.3V)) and guaranteed monotonicity over a wide supply-voltage range. It is an ideal part for applications in contrast/brightness control or voltage adjustment in feedback loops.

Description

The LTC1427-50 communicates with external circuitry using the standard 2-wire I²C or SMBus interface. The operating sequence (Figure 1) shows the signals on the SMBus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors are required on these lines. The LTC1427-50 is a receive-only (slave) device; the system master must apply the Write Byte protocol (Figure 1) to communicate with the LTC1427-50.

The master places the LTC1427-50 in a START condition and transmits a 7-bit address. The write bit is then made 0. The LTC1427-50 acknowledges and the master transmits the command byte. The LTC1427 again acknowledges and latches the active bits of the command byte into register A (see the block diagram in Figure 2) at the falling edge of the acknowledge pulse. The master then sends the data byte; the LTC1427-50 acknowledges receipt of the data byte; and, finally, the 8-bit data byte and the last two output bits (the two MSBs of the 10-bit input data) from register A are latched into the register C at the falling edge of the final acknowledge and the DAC current output assumes the new 10-bit value. A stop condition is optional.

The LTC1427-50 can respond to one of four 7-bit addresses. The first five bits have been factory programmed and are always 01011. The last two LSB address bits are programmed by the user via AD1 and AD0 (Table 1). When AD1 and AD0 are both connected to V_{CC}, upon power up, the 10-bit internal register C is reset to 1000000000B and the DAC output is set to midrange. If either AD1 or AD0 is connected to ground, at power-up, register C resets to 0000000000B and the DAC output is set to zero. For the LTC1427-50, the source current output (I_{OUT}) can be biased from –15V to (V_{CC} – 1.3V); precision full-scale current is trimmed to ±1.5% at room temperature and ±2.5% over the commercial temperature range.

There are two ways to shut down the LTC1427 (see Figure 2). A logic low at the $\overline{SHDN}$ pin or a logic high at bit 7 of the command byte sent through the SMBus interface will put the LTC1427 into shutdown mode. In shutdown mode, the digital data is retained internally and the supply current drops to only 12µA typically.

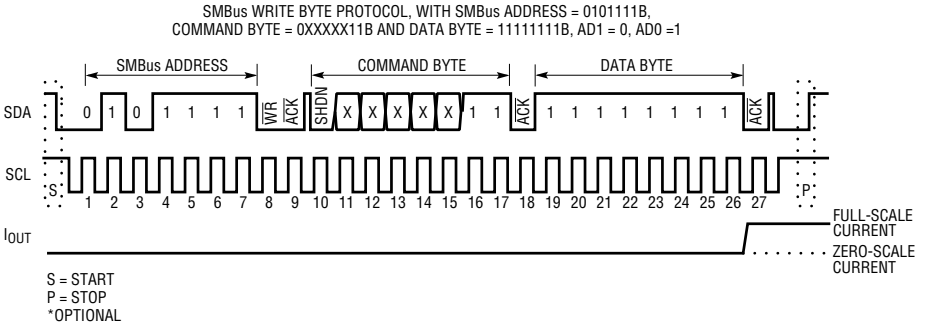

Figure 1. LTC1427-50 operating sequence

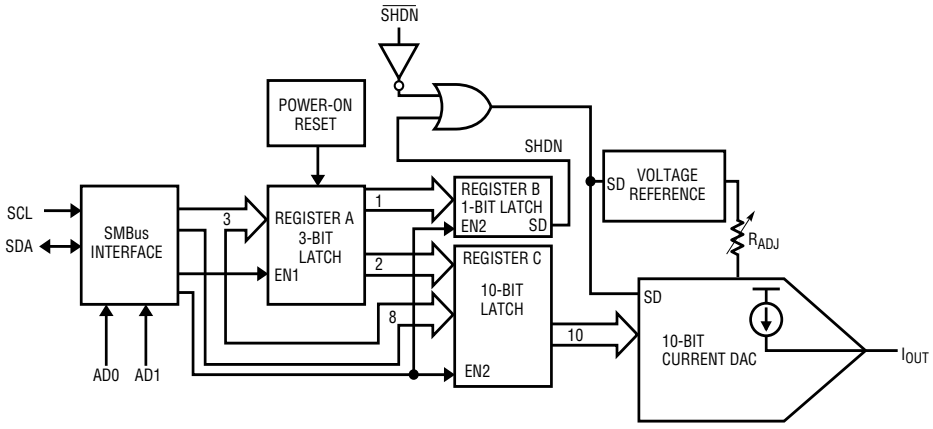

Figure 2. LTC1427-50 block diagram

Table 1. LTC1427-50 function table

AD1	AD0	SMBus Address Location	DAC Power-Up Value	Application
L	L	0101101	Zero-scale	LCD Backlight Control
L	H	0101111	Zero-scale	General Purpose
H	L	0101110	Zero-scale	General Purpose
H	H	0101100	Mid-scale	LCD Contrast Control

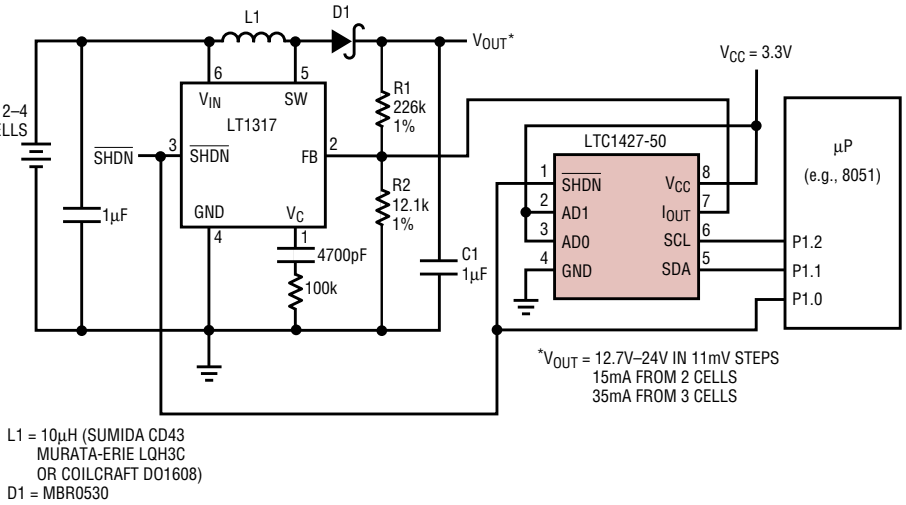

Figure 3. Digitally controlled LCD bias generator

Digitally Controlled LCD Bias Generator

Figure 3 is a schematic of a digitally controlled LCD bias generator using a standard SMBus 2-wire interface. The LT1317 is configured as a boost converter, with the output voltage (V_{OUT}) determined by the values of the feedback resistors, R1 and R2. The LTC1427-50's DAC current output is connected to the feedback node of the LT1317. The LTC1427-50's DAC current output increases or decreases according to the data sent via the SMBus. As the DAC output current varies from 0µA to 50µA, the output voltage is controlled over the range of 12.7V to 24V. A 1LSB change in the DAC output current corresponds to an 11mV change in the output voltage.

Digitally Controlled CCFL Current Using the SMBus Interface

Figure 4 is a schematic of a 90% efficient, digitally controlled floating CCFL lamp supply using the SMBus serial interface. The DAC current output is connected to the I_{CCFL} pin of LT1184F. With the DAC output current range of 0µA to 50µA, this circuit gives 0mA to 6mA lamp current for a typical display. Varying the lamp current from its minimum to maximum level adjusts the lamp intensity, and hence, the display brightness.

Conclusion

The LTC1427-50 is a precision 10-bit, 50µA full-scale DAC that communicates directly with an I^2C or SMBus interface. It operates from a wide supply range, consumes low power, has guaranteed monotonicity and is packaged in a popular SO-8. It is ideal for applications such as contrast/brightness controls, output voltage adjustment in power supplies and other potentiometer applications.

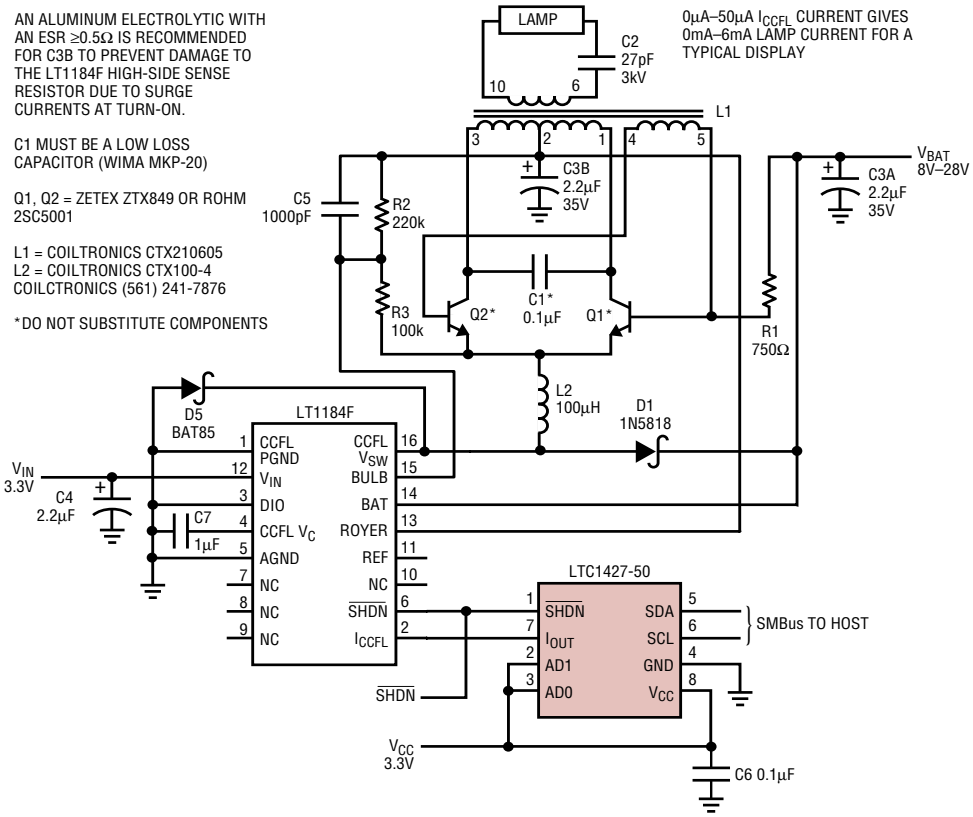

Figure 4. 90% efficient digitally controlled floating CCFL supply using the SMBus serial interface

Micropower 600kHz Fixed-Frequency DC/DC Converters Step Up from a 1-Cell or 2-Cell Battery

by Steve Pietkiewicz

Linear Technology introduces two new micropower DC/DC converters designed to provide power from a single-cell or higher input voltage. The LT1308 features an onboard switch capable of handling 2A with a voltage drop of 300mV and operates from an input voltage as low as 1V. The LT1317, intended for lower power requirements, operates from an input voltage as low as 1.5V. Its internal switch handles 600mA with a drop of 360mV. Both devices feature Burst Mode operation at light load; efficiencies are above 70% for load currents of 1mA. Both devices switch at 600kHz; this high frequency keeps associated power components small and flat; additionally, troublesome interference problems in the sensitive 455kHz IF band are avoided. The LT1308 is intended for generating power on the order of 2W–5W. This is sufficient for RF power amplifiers in GSM or DECT terminals or for digital-camera power supplies. The LT1317, with its smaller switch, can generate 100mW to 2W of power. The LT1317 is available in LTC's smallest 8-lead package, the MSOP. This package is approximately one-half the size of a standard 8-lead SO package. The LT1308 is available in the 8-lead SO package.

Single Li-Ion Cell to 5V/1A DC/DC Converter for GSM

GSM terminals have emerged as a worldwide standard. A common requirement for these products is an efficient, compact, step-up converter to develop 5V from a single Li-Ion cell to power the RF amplifier. The LT1308 performs this function with a minimum of external components. The circuit is detailed in Figure 1. Many designs use a large aluminum electrolytic capacitor (1000µF to 3300µF) at the DC/DC converter output to hold up the output voltage during the transmit time slice, since the amplifier can require more than 1A. The

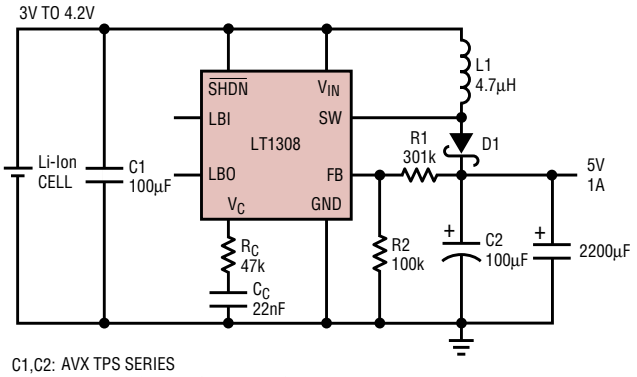

Figure 1. Single Li-Ion cell to 5V/1A DC/DC converter

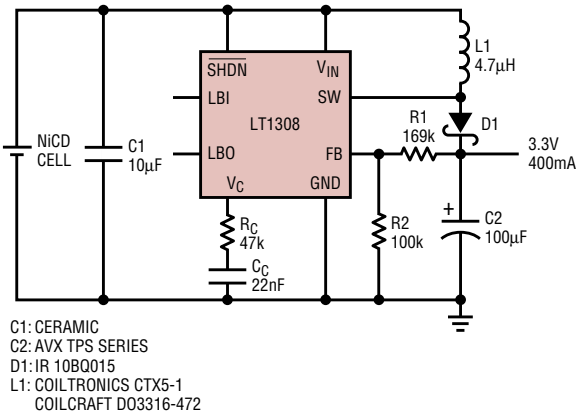

Figure 4. Single NiCd cell to 3.3V/400mA DC/DC converter

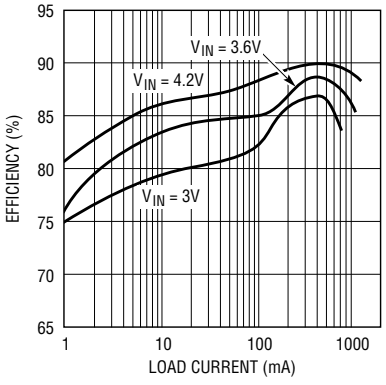

Figure 2. Efficiency of Figure 1's circuit reaches 90%

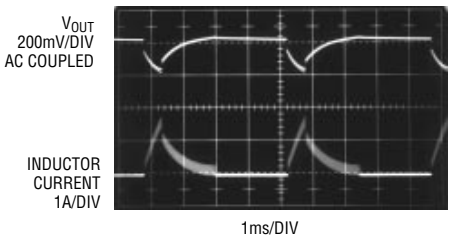

Figure 3. Transient response of DC/DC converter: V_{IN} = 3V, 0A–1A load step

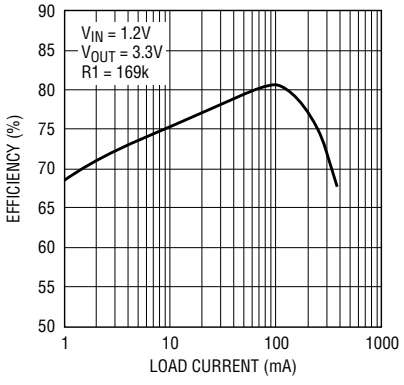

Figure 5. Efficiency of Figure 4's circuit reaches 81%

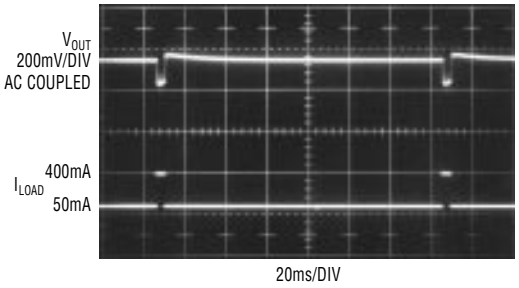

Figure 6. DECT load transient response: with a single NiCd cell, the LT1308 provides 3.3V with a 400mA pulsed load. The pulse width = 416µs.

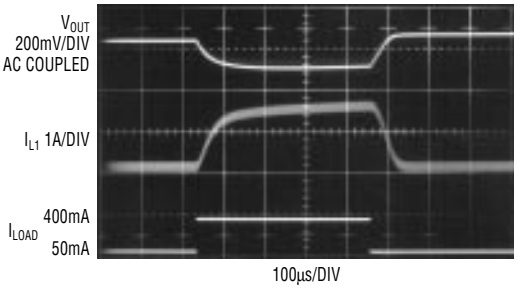

Figure 7. DECT load transient response: faster sweep speed (100µs/DIV) details V_{OUT} and inductor current of a single DECT transmit pulse.

output capacitor, along with the LT1308 compensation network, serves to smooth out the input current demanded from the Li-Ion cell. Efficiency, which reaches 90%, is shown in Figure 2. Transient response of a 0A to 1A load step with typical GSM profiling (1:8 duty cycle, 577µs pulse duration) is depicted in Figure 3. Voltage droop (top trace) is 200mV. Inductor current (bottom trace) increases to 1.7A peak; the input capacitor supplies some of this current, with the remainder drawn from the Li-Ion cell.

Single NiCd Cell to 3.3V/ 400mA Supply for DECT

Only minor changes are required in Figure 1's circuit to construct a single-cell NiCd to 3.3V converter. The large output capacitor is no longer required as the output current can be handled directly by the LT1308. Figure 4 shows the DECT DC/DC converter circuit. Efficiency, reaching 81% from a 1.2V input, is pictured in Figure 5. Transient response of a typical DECT load of 50mA to 400mA is detailed in Figure 6. Output voltage droop (top trace) is under 200mV. Figure 7 zooms in on a single pulse to show the output voltage and inductor current responses more clearly.

2-Cell Digital Camera Supply Produces 3.3V, 5V, 18V and –10V

Power supplies for digital cameras must be small and efficient while generating several voltages. The DSP and logic need 3.3V, the ADC and LCD display need 5V and biasing for the CCD element requires 18V and –10V. The power supplies must also be free of low frequency noise, so that postfiltering can be done easily. The obvious approach, to use a separate DC/DC converter IC for each output voltage, is not cost-effective. A single LT1308, along with an inexpensive transformer, generates 3.3V/200mA, 5V/200mA, 18V/10mA and –10V/10mA from a pair of AA or AAA cells. Figure 8 shows the circuit. A coupled-flyback scheme is used, actually an extension of the SEPIC (single ended primary inductance converter) topology. The addition of capacitor C6 clamps the SW pin, eliminating a snubber network. Both the 3.3V and 5V outputs are fed back to the LT1308 FB pin, a technique known as split feedback. This compromise results in better overall line and load regulation. The 5V output has more influence than the 3.3V output, as can be seen from the relative values of R2 and R3. Transformer T1 is available from Coiltronics, Inc. (561-241-7876). Efficiency vs input voltage for several load currents on both 3.3V and 5V outputs is pictured in Figure 9. The CCD bias voltages are loaded with 10mA in all cases.

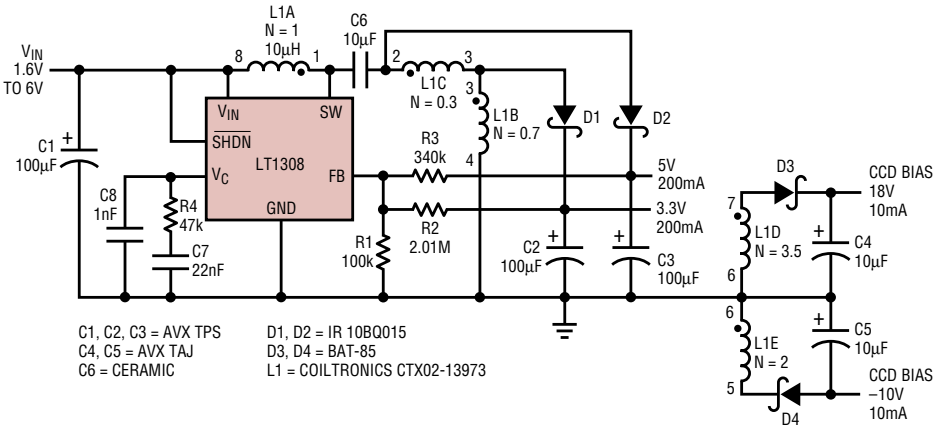

Figure 8. This digital camera power supply delivers 5V/200mA, 3.3V/200mA, 18V/ 10mA and –10V/10mA from two AA cells.

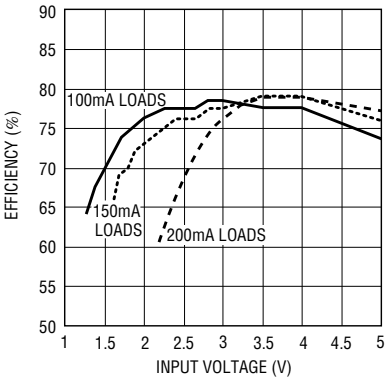

Figure 9. Camera power supply efficiency reaches 78%.

LT1317 2-Cell to 5V DC/DC Converter

Figure 10 shows a simple 2-cell to 5V DC/DC converter using the LT1317. This device generates a clean, low ripple output from an input voltage as low as 1.5V. Designed for 2-cell applications, it offers better performance than its 1-cell predecessor, the LT1307. More gain in the error amplifier results in lower Burst Mode ripple, and an internal preregulator eliminates oscillator variation with input voltage. For comparison, Figure 11 details transient responses of both the LT1307 and the LT1317 generating 5V from a 3V input. The load step is 5mA to 200mA. Output capacitance in both cases is 33µF. The LT1307 has low frequency ripple of 100mV, whereas the LT1317 Burst Mode ripple of 20mV is the same as the 600kHz ripple resulting from the output capacitor's ESR with a 200mA load.

Single Li-Ion Cell to ±4V DC/DC Converter

By again employing the SEPIC topology, a ±4V supply can be designed with one IC. Figure 12's circuit generates 4V at 70mA and –4V at 10mA from an input voltage ranging from 2.5V to over 5V. Maximum component height is 2mm. This converter uses two separate inductors (L1 and L2), so it is an uncoupled SEPIC converter. This reduces the overall cost, but requires that all output current pass through C1. Since C1 is ceramic, its ESR is low and there is no appreciable efficiency loss. C5 is charged to $-V_{OUT}$ when the switch is off, then its bottom plate is grounded when the switch turns on. The negative output is fairly well regulated, since the diode drops tend to cancel. The circuit is switching continuously at rated load, where efficiency is 75%. Output ripple is under 40mV and can be reduced further with conventional postfiltering techniques.

Conclusion

The LT1308 and LT1317 provide low noise compact solutions for contemporary portable-product power supplies.

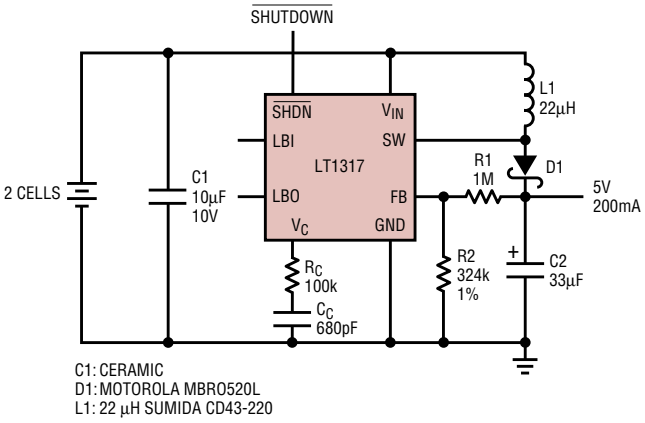

Figure 10. 2-cell to 5V boost converter using the LT1317

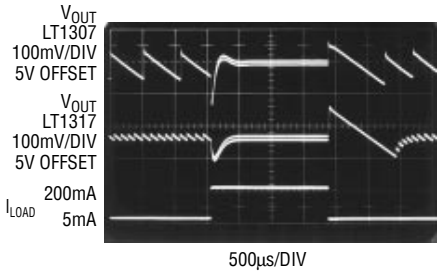

Figure 11. The LT1317 has reduced Burst Mode ripple compared to the LT1307.

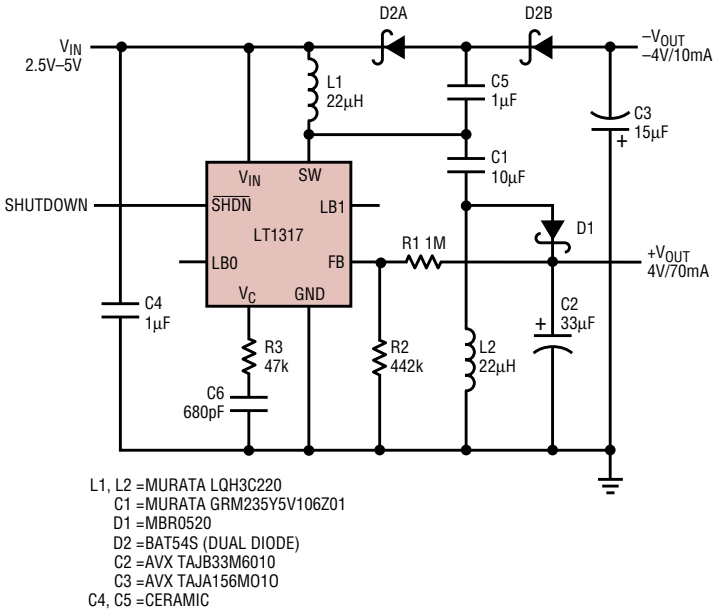

Figure 12. This single Li-Ion cell to ±4V DC/DC converter has a maximum height of 2mm.

New 333ksps, 16-Bit ADC Offers 90dB SINAD and –100dB THD

by Marco Pan

The fastest, highest performance 16-bit sampling ADC is now available in a tiny 36-pin SSOP package from Linear Technology. It is the LTC1604. This device runs at 333ksps and delivers excellent DC and AC performance. The LTC1604 operates on ±5V supplies and typically draws only 220mW. It is a complete differential, high speed, low power, 16-bit sampling ADC that requires no external components. The LTC1604 also provides two power shutdown modes, NAP and SLEEP, to reduce power consumption during inactive periods. This 333ksps, 16-bit device not only offers the performance of the best hybrids but also provides low power, small size, an easy-to-use interface and the low cost of a monolithic part. Some of the key features of this new device include:

- ❏ 333ksps throughput
- ❏ 16 bits with no missing codes and ±2LSB INL
- ❏ Low power dissipation and power shutdown
- ❏ Excellent AC and DC performance
- ❏ Small package—36-pin SSOP

These features of the LTC1604 can simplify, improve, and lower the cost of current data acquisition systems and open up new applications that were not previously possible because no similar part was available.

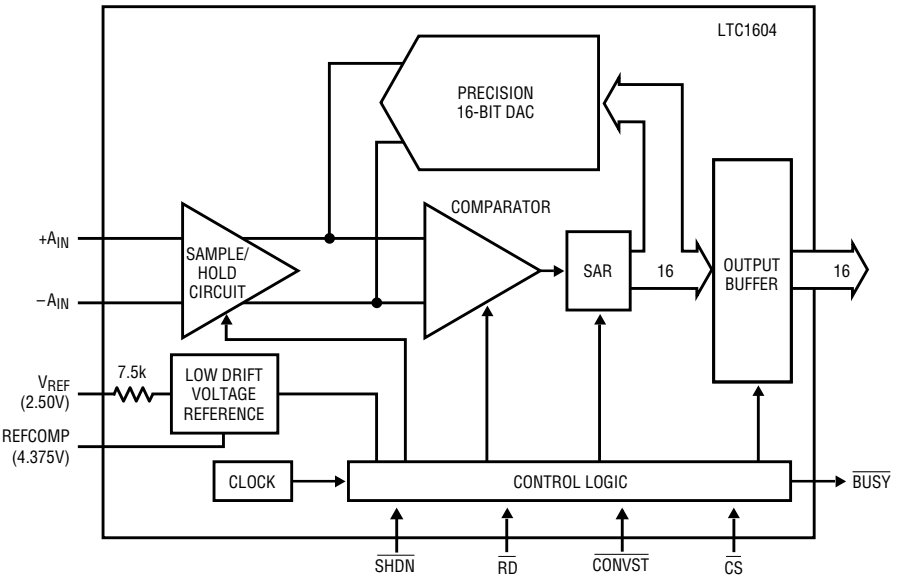

Figure 1. LTC1604 block diagram

Fast Architecture

To achieve 333ksps with outstanding AC and DC performance at the 16-bit level, careful design is required. Figure 1, the LTC1604 block diagram, illustrates the design of this part. A high performance differential sample-and-hold circuit, combined with an extremely fast successive-approximation ADC and an on-chip reference, delivers an excellent combination of AC and DC performance. A digital interface allows easy connection to microprocessors, FIFOs or DSPs.

Outstanding AC and DC Performance

The DC specifications include 16 bits with no missing codes and ±2LSB integral nonlinearity error guaranteed over temperature. The gain of the ADC is held nearly constant over temperature with an on-chip 10ppm/°C (typical) curvature-corrected bandgap reference. Figures 2 and 3 show INL and DNL error plots, respectively, for the LTC1604.

The sample-and-hold circuit determines the dynamic performance of the ADC. The LTC1604 has a wide bandwidth, very low distortion, differential sample-and-hold. Fast Fourier transform (FFT) test techniques are used to test the LTC1604's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral

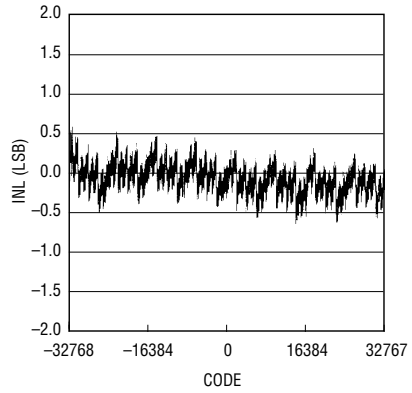

Figure 2. The LTC1604 is very accurate, as shown in the INL error plot. This accuracy is achieved without autocalibration and its associated overhead. Accuracy relies on capacitor matching, which is very stable over temperature and time.

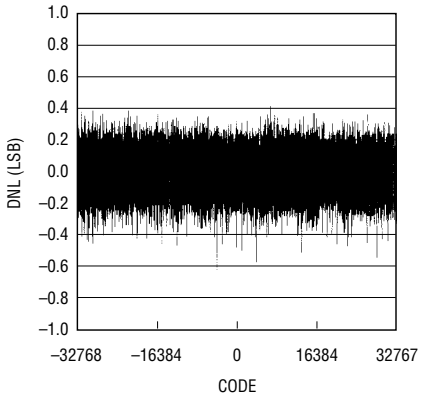

Figure 3. The differential nonlinearity error plot shows the excellent performance of the LTC1604.

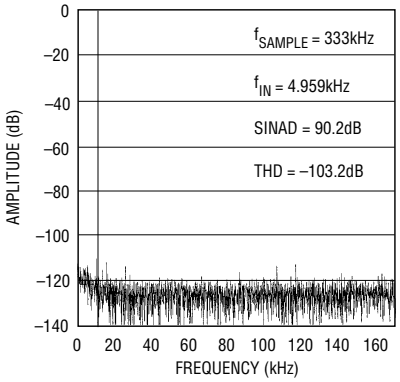

Figure 4. This FFT of the LTC1604's conversion of a full-scale 5kHz sine wave shows outstanding response with a very low noise floor when sampling at 333ksps.

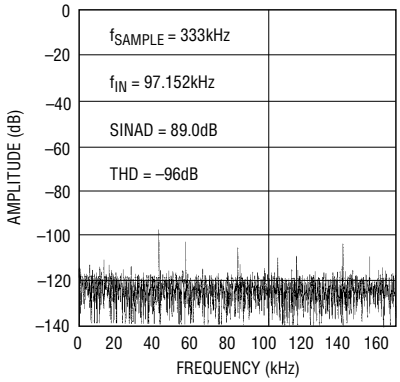

Figure 5. Even with inputs at 100kHz, the LTC1604's dynamic linearity remains robust.

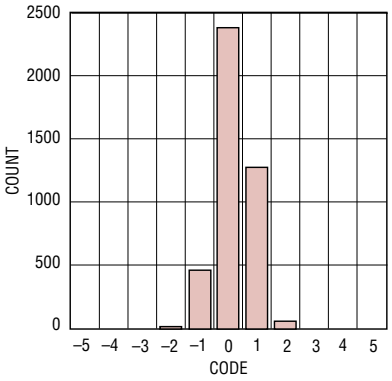

Figure 6. This histogram shows that the LTC1604 has an RMS code transition noise of 0.66dB.

content can be examined for frequencies other than the fundamental. Figures 4 and 5 show the excellent AC performance of the LTC1604 at 333ksps with f_{IN} = 5kHz and 100kHz, respectively. The AC performance of the LTC1604 include total harmonic distortion of –100dB for a 5kHz input and –94dB for a 100kHz input and an input bandwidth of 15MHz for the sample-and-hold.

Very Low Noise

The noise of an ADC can be evaluated in two ways: by signal-to-noise ratio (SNR) in the frequency domain and by histogram in the time domain. The LTC1604 excels in both. Figure 4 demonstrates that the LTC1604 has a SNR of over 90dB in the frequency domain. The noise in the time-domain histogram is the transition noise associated with a high resolution ADC, which can be measured with a fixed DC signal applied to the input of the ADC. The resulting output codes are collected over a large number of conversions. The shape of the distribution of codes will give an indication of the magnitude of the transition noise. In Figure 6, the distribution of output codes is shown for a DC input that has been digitized 4096 times. The distribution is Gaussian and the RMS code transition noise is about 0.66LSB. This corresponds to a noise level of 90.9dB relative to full scale. When added to the theoretical 98dB of quantization error for a 16-bit ADC, this yields an SNR of 90.1dB, which correlates very well with the frequency domain measurements.

Differential Inputs Ignore Common Mode Noise

Getting a clean signal to the input(s) of an ADC, especially a 16-bit ADC, is not an easy task in many systems. Large noise signals from EMI, the AC power line and digital circuitry are usually present. Filtering and shielding are the common techniques for reducing noise, but these are not always adequate (see "The Care and Feeding of High Performance ADCs: Getting All the Bits You Paid For"; *Linear Technology* VI:3 [August, 1996]). The LTC1604 offers another tool to fight noise: differential inputs.

Figure 7a depicts a typical single-ended sampling system with ground noise, which may be 60Hz noise, digital clock noise or some other type of noise. When a single-ended input is used, the ground noise adds directly to the input signal. By using the differential inputs of the LTC1604 the ground noise can be rejected by connecting the inputs directly across the signal of interest, as shown in Figure 7b. Ground noise becomes "common mode" and is rejected internally by the LTC1604 by virtue of its excellent common mode rejection ratio (CMRR). Figure 8 shows the CMRR of the LTC1604 versus frequency. Notice that the CMRR is constant over the entire Nyquist bandwidth and is only 6dB lower at 300kHz. This ability to reject high frequency common mode signals is very helpful in sampling systems, where noise often has high frequency components due to switching transients.

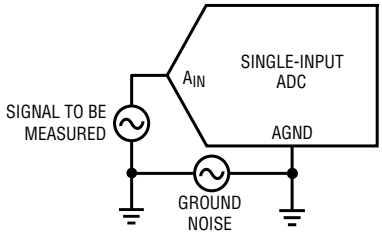

Figure 7a. Single-input ADC measuring a signal riding on common mode noise.

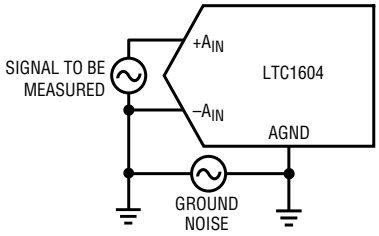

Figure 7b. Differential-input ADC measuring a signal riding on common mode noise.

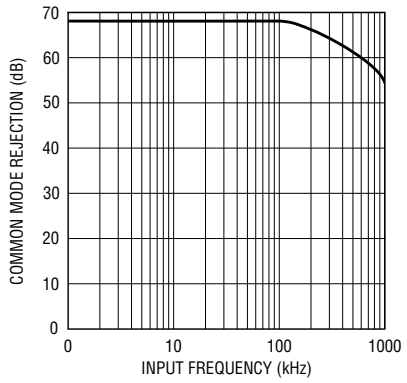

Figure 8. LTC1604 CMRR vs frequency

3V Input/Output Compatible

The LTC1604 operates on ±5V supplies, which makes the device easy to interface to 5V digital systems. This device can also talk to 3V digital systems: the digital input pins ($\overline{SHDN}$, $\overline{CS}$, $\overline{CONVST}$ and $\overline{RD}$) of the LTC1604 recognize 3V or 5V inputs. The LTC1604 has a dedicated output supply pin (OV_{DD}) that controls the output swings of the digital output pins (D0–D15, $\overline{BUSY}$) and allows the part to talk to either 3V or 5V digital systems.

Low Power Dissipation and Shutdown

The LTC1604 runs at full speed on ±5V supplies and typically draws only 220mW. This power consumption can be reduced further by using the two power shutdown modes, NAP and SLEEP, during inactive periods. NAP mode cuts down the power to 8mW, leaving the reference and logic powered up. The ADC wakes up "instantly" (400ns) from NAP mode, so NAP mode can be invoked even during brief inactive periods with no penalty or delay when conversions must start again.

SLEEP mode is used when there are extended inactive periods. In SLEEP mode, the ADC powers down all the circuitry, leaving the logic outputs in a high impedance state. The only current that remains is junction-leakage current (less than 1µA). It takes much longer for the ADC to wake up from SLEEP mode because the reference circuit must power up and settle to 0.0006% for full accuracy. The wake-up time also depends on the value of the compensation capacitor used on the REF COMP pin. With the recommended 47µF capacitor, the wake-up time is 160ms.

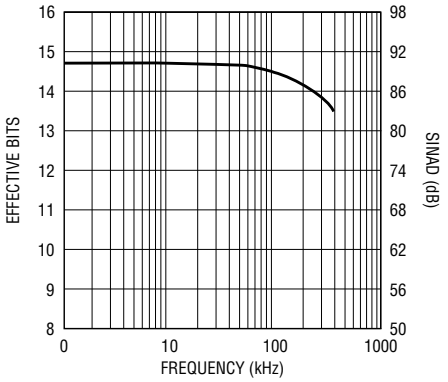

Figure 9. The LTC1604 has essentially flat SINAD and effective bits out to Nyquist.

Applications

The performance of the LTC1604 makes it very attractive to use in a wide variety of applications, such as digital signal processing, PC data acquisition cards, medical instrumentation and high resolution or multiplexed data acquisition.

DSP applications often require excellent dynamic performance, since the ADC must sample high frequency AC signals. The LTC1604 is the right choice in these types of applications because of the performance of its sample-and-hold. Figure 9 shows how well the signal-to-noise plus distortion ratio and the spurious free dynamic range of the converter hold up as the input frequency is increased.

Another common application is PC data acquisition cards. The high sample rate, the simple, complete configuration and excellent linearity of the LTC1604 make it an ideal choice here. Another advantage that the LTC1604 provides is the synchronized internal conversion clock, which is very useful in this application. This feature eliminates the second external clock required by other sampling ADCs to run conversion, in addition to the normal sample signal. Clearly, this feature makes the LTC1604 an outstanding choice for PC data acquisition cards.

For single-channel or multiplexed high speed data acquisition systems, the LTC1604 has the high sample rate and high impedance inputs that help smooth the design of these applications. High sample rates allow more channels in the data acquisition system on a very low power and cost budget and the high impedance inputs of the ADC make them very easy to multiplex.

Conclusion

The new LTC1604 is a complete 16-bit ADC with a built-in sample-and-hold and reference. It samples at 333ksps and is the fastest device of its kind on the market. The excellent DC and AC performance of the LTC1604 not only make it extremely valuable in a wide variety of existing high resolution applications while also opening up new applications.

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Ultralow Power 14-Bit ADC Samples at 200ksps

by Dave Thomas

Introduction

A new, versatile 14-bit ADC, the LTC1418, can digitize at 200ksps while consuming only 15mW from a single 5V supply. The LTC1418 is designed to be easy to use and adaptable, requiring little or no support circuitry in a wide variety of applications. Some of the key features of this new device include:

- ❏ 200ksps throughput
- ❏ Low power—15mW
- ❏ Single 5V or ±5V supplies
- ❏ 1.25LSB INL max and 1LSB DNL max
- ❏ Parallel and serial data output modes
- ❏ NAP and SLEEP power shutdown modes
- ❏ Small package—28-pin SSOP

High Performance without High Power

Figure 1 shows a block diagram of the LTC1418. This device includes a high performance differential sample-and-hold circuit, an ultra-efficient successive approximation ADC, an on-chip reference and a digital interface that allows easy serial or parallel interface to a microprocessor, FIFO or DSP. The LTC1418 is factory calibrated, so a lengthy calibration cycle is not required to achieve 14-bit performance. DC specifications include a 1LSB max differential linearity error (no missing codes) and 1.25LSB max integral linearity error guaranteed over temperature. The gain of the ADC is controlled by an on-chip 10ppm/°C reference that can be easily overdriven with an external reference if required.

For AC applications, the dynamic performance of the LTC1418 is exceptional. The extremely low distortion differential sample-and-hold acquires input signals at frequencies up to 10MHz. At the Nyquist frequency, 100kHz, the spurious free dynamic range is typically 95dB. The noise is also low with a signal-to-noise ratio (SNR) of 82dB from DC to well beyond Nyquist.

The superior AC and DC performance of the LTC1418 doesn't require a lot of power. In fact, the LTC1418 has the lowest power of any 14-bit ADC available, just 15mW at 200kHz (10mW at sample rates below 50kHz). Two shutdown modes make it possible to cut power further at lower sample rates.

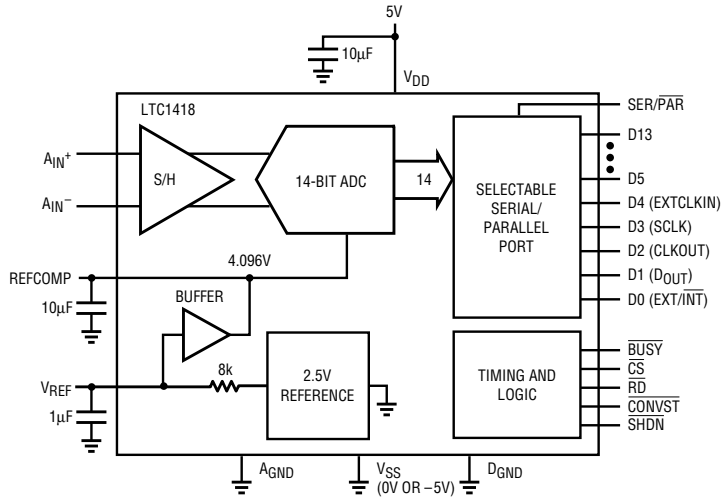

Figure 1. LTC1418 block diagram

High Impedance Inputs

The LTC1418's high impedance inputs allow direct connection of high impedance sources without introducing errors. Many ADCs have a resistive input or input bias current that requires low source impedance to achieve low errors. Other ADCs with switched capacitor inputs exhibit large offset shifts when driven with high source impedance or a large source-impedance imbalance between their differential inputs. The unique sample-and-hold circuit of the LTC1418 has a low capacitance, high resistance (10MΩ||25pF) switched-capacitor input that has only 2LSB of offset shift with a source impedance imbalance between 0Ω and 1M (see Figure 2a). (There is no shift if the input impedance is equal for $+A_{IN}$ and

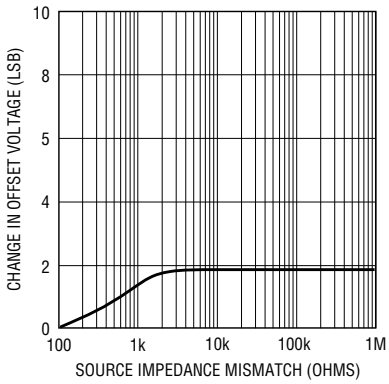

Figure 2a. Change in offset voltage with source impedance mismatch

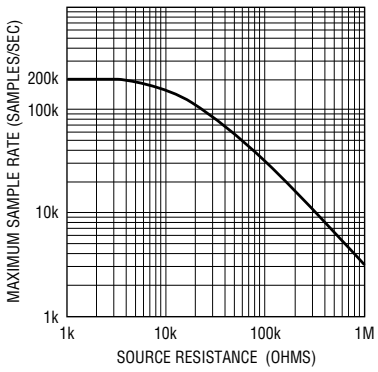

Figure 2b. Maximum sample rate vs unbuffered source resistance

$-A_{IN}$.) Connecting the ADC directly to a high impedance source avoids additional noise and offset errors that may be introduced by buffering circuitry. The only downside to directly connecting the ADC to a high source impedance is that the acquisition time will increase. The low input capacitance (20pF) of the LTC1418 allows full-speed operation with resistances up to 2k. Above 2k the sample rate must be lowered (see Figure 2b).

Differential Inputs with Wideband CMRR

The differential input of the LTC1418 has excellent common mode rejection, eliminating the need for some input-conditioning circuitry. Op amps and instrumentation amplifiers are often used to reject common mode noise from EMI, AC power and switching noise. Although these circuits perform well at low frequencies, their rejection at high frequencies deteriorates substantially. Figure 3 shows the CMRR of the LTC1418 vs frequency.

Single-Supply or Dual-Supply Operation

Single-supply ADCs can be cumbersome to work with in a dual-supply system. A signal with a common mode of zero volts has to be shifted up to the common mode of the ADC. Shifting the common mode can be accomplished with AC coupling, but DC information is lost. Alternatively, an op amp level shifter can be used, but this adds circuit complexity and additional errors. The LTC1418 can operate with single or dual supplies and allows direct coupling to the inputs in both cases. The ADC is equipped with circuitry that automatically detects when –5V is present at the V_{SS} pin. With a –5V supply, the ADC operates in bipolar mode and the full-scale range becomes ±2.048V for $+A_{IN}$ with respect to $-A_{IN}$. With a single supply, V_{SS} = 0V and the ADC operates in unipolar mode with an input range of 0V to 4.096V.

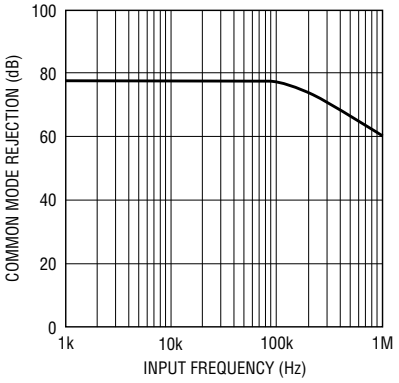

Figure 3. Input common mode rejection vs input frequency

On-Chip Reference

The on-chip reference of the LTC1418 is a standard 2.5V and is compatible with many system references; it is available on the REF output (pin 3). An internal amplifier boosts the 2.5V reference up to 4.096V; this sets the span for the ADC. The 4.096V output is available on the REFCOMP output (pin4) and may be used as a reference for other external circuitry. With a temperature coefficient of 10ppm/°C, both REF and REFCOMP are suited to serve as the master reference for the system. However, if an external reference circuit is required, its easy to overdrive either reference output. The 2.5V reference output is resistive (4k) and can be easily overdriven by any reference with low output impedance by directly connecting the external reference to the REF pin. If REFCOMP (the 4.096V reference) is to be overdriven, tie the REF pin to ground. This disables the output drive of the REFCOMP amplifier, allowing it to be easily overdriven.

Parallel Data Output for High Speed

The parallel output mode of the LTC1418 allows the lowest digital overhead. A microcontroller can strobe the ADC to start the conversion and perform other tasks while the conversion is running. The ADC will then signal the microcontroller after the conversion is complete with the $\overline{BUSY}$ signal, at which time valid data is available on the parallel output bus. $\overline{BUSY}$ may also be used to clock latches or a FIFO directly, since data is guaranteed to be valid with the rising edge of $\overline{BUSY}$.

Serial Data Output for Minimal Wiring

The serial output mode of the LTC1418 is simple, requiring just three pins for data transfer: a data-out pin, a serial clock pin and a control pin. However, its simplicity doesn't sacrifice flexibility. Serial data can be clocked with the internal shift clock for minimal hardware or an external shift clock for synchronization. Additionally, data can be clocked out during the conversion for the highest throughput rate or after the conversion for maximum noise immunity.

Perfect for Telecom: Wide Dynamic Range

Telecommunications systems require wide dynamic range. With its low noise and low distortion, the LTC1418 offers extremely wide dynamic range over its entire Nyquist bandwidth. Spurious free dynamic range is typically 95dB and only starts to drop off at input frequencies above Nyquist. The ultralow jitter of the sample-and-hold circuit, $5ps_{RMS}$, keeps the SNR flat from DC to 1MHz, making this device useful for undersampling applications.

Another important requirement for telecom systems is a low error rate. In any ADC, there is a finite probability that a large conversion error (greater than 1% of full scale) will occur. In video or flash converters, these large errors are called "sparkle codes." Large errors are a problem in telecom systems such as ISDN, because they result in errors in data transmission. All ADCs have a rate at which errors occur, referred to as the error rate. The error rate is dependent on the ADC architecture, design and process. Error rates vary greatly and can be as low as 1 in 10 billion to as high as 1 is 1 million. Telecom systems typically require error rates to be 1 in 1 billion or better.

The LTC1418 is designed to have ultralow error rates. The error rate is so low that it is difficult to measure because of the time in between errors. To make measurement more practical, the error rate was measured at an elevated temperature of 150°C,

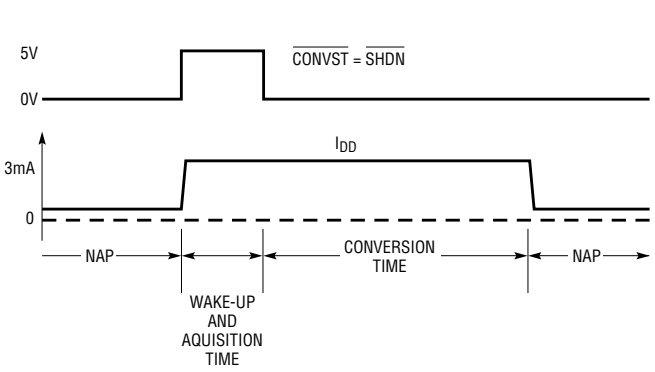

Figure 4a. NAP mode between conversions

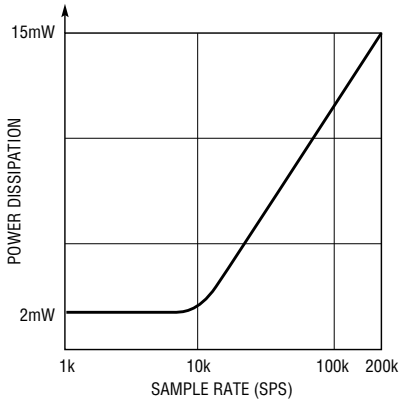

Figure 4b. Power dissipation vs sample rate with NAP mode between conversions

because error rate increases with temperature. Even at this high temperature, the error rate was 1 in 100 billion. The projected error rate at room temperature is 1 in 2,000,000 billion or about 1 error every 320 years if running at full conversion rate.

Ideal for Low Power Applications

LTC1418 is especially well suited for applications that require low power and high speed. The normal operating power is low—only 15mW. Power may be further reduced if there are extended periods of time between conversions. During these inactive periods when the ADC is not converting, the LTC1418 may be shut down. There are two power shutdown modes: NAP and SLEEP.

NAP mode shuts down 85% of the power and leaves only the reference and logic powered up. The LTC1418 can wake up from NAP mode very quickly; in just 500ns it can be ready to start converting. In NAP mode, all data-output control is functional; data from the last conversion prior to starting NAP mode can be read during NAP mode. $\overline{RD}$ also controls the state of the output buffers. NAP mode is useful for applications that must be ready to immediately take data after long inactive periods.

With slow sample rates, power can be saved by automatically invoking NAP mode between conversions. Referring to Figure 4, the $\overline{SHDN}$ pin and $\overline{CONVST}$ pin are driven together. A conversion will be started with the falling edge of this signal; once the conversion is completed, the ADC will automatically shut down. Before the next conversion can start, the $\overline{CONVST}$ and $\overline{SHDN}$ pins must be brought high early enough to allow for the 500ns wake-up time. Power drops with the sample frequency until it approaches the power of the reference circuit, about 2mW at frequencies less than 10kHz.

The SLEEP mode is used when the NAP-mode current drain is too high or if wake-up time is not critical. In SLEEP mode, all bias currents are shut down, the reference is shut down and the logic outputs are put in a high impedance state. The only current that remains is junction leakage current, less than 1µA. Wake-up from the SLEEP mode is much slower, since the reference circuit must power up and settle to 0.01% for full accuracy. The wake-up time is also dependent on the value of the compensation capacitor used on the REFCOMP pin; with the recommended 10µF capacitor the wake up time is 10ms. SLEEP mode is useful for long inactive periods, that is, times greater than 10ms.

Conclusion

The new LTC1418 low power, 14-bit ADC will find uses in many types of applications, from industrial instrumentation to telephony. The LTC1418's adaptable design reduces the need for expensive support circuitry. This can result in a smaller, lower cost system.

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A 10MB/s Multiple-Protocol Chip Set Supports Net1 and Net2 Standards

by David Soo

Introduction

With the increase in multinational computer networks comes the need for the network equipment to support different serial protocols. One solution is to provide a different serial interface board for each market. This can become unmanageable as product volume increases. The issues of board swapping and inventory are often discounted. Another solution is to place all of the serial interfaces, each isolated, on a single board. For example, when the product is sold with V.35, the serial cable is mapped to that section of the board. This requires a large connector plus signal routing and board space.

The best solution is to support many different serial protocols on one connector, but that requires the circuitry for each serial protocol to share the same connector pins. At first glance this may not appear to be difficult. Further examination reveals conflicting line-termination standards that require resistors to be switched to the connector pins. As the designer becomes occupied with the details of the interface specification, there is always the possibility that one small detail will be missed. This compliance headache causes designers to seek out a cost-effective integrated solution.

With the LTC1543, LTC1544 and LTC1344A, LTC has taken the integrated approach to multiple-protocol. It does not make sense to use a handful of standard interface parts when Net1 and Net2 compliance is guaranteed with the LTC1543, LTC1544 and LTC1344A. Detecon, Inc. documents this compliance in Test Report No. NET2/102201/97. With this chip set, network designers can concentrate on functions that increase the end-product value rather than on standards compliance.

Typical Application

Like the LTC1343 software-selectable multiprotocol transceiver, introduced in the August, 1996 issue of *Linear Technology*, the LTC1543/LTC1544/LTC1344A chip set creates a complete software-selectable serial interface using an inexpensive DB-25 connector. The main difference between these parts is the division of functions: the LTC1343 can be configured as a data/clock chip or as a control-signal chip using the CTRL/CLK pin, whereas the LTC1543 is a dedicated data/clock chip and the LTC1544 is a control-signal chip. The chip set supports the V.28 (RS232), V.35, V.36, RS449, EIA-530, EIA-530A and X.21 protocols in either DTE or DCE mode.

Figure 1 shows a typical application using the LTC1543, LTC1544 and LTC1344A. By just mapping the chip pins to the connector, the design of the interface port is complete. The figure shows a DCE mode connection to a DB-25 connector.

The LTC1543 contains three drivers and three receivers, whereas the LTC1544 contains four drivers and four receivers. The LTC1344A contains six switchable resistive terminators that are connected only to the high speed clock and data signals. When the interface protocol is changed via the mode selection pins, M2, M1 and M0, the drivers, receivers and line terminators are placed in their proper configuration. The mode pin functions are summarized in Table 1. There are internal 50µA pull-up current sources on the mode select pins, DCE/DTE and the INVERT pins.

Table 1. Mode pin functions

LTC1543/LTC1544 Mode Name	M2	M1	M0
Not Used	0	0	0
EIA-530A	0	0	1
EIA-530	0	1	0
X.21	0	1	1
V.35	1	0	0
RS449/V.36	1	0	1
RS232/V.28	1	1	0
No Cable	1	1	1

DTE vs DCE Operation

The LTC1543/LTC1544/LTC1344A chip set can be configured for either DTE or DCE operation in one of two ways. The first way is when the chip set is a dedicated DTE or DCE port with a connector of appropriate gender. The second way is when the port has one connector that can be configured for DTE or DCE operation by rerouting the signals to the chip set using a dedicated DTE or DCE cable.

Figure 1 is an example of a dedicated DCE port using a female DB-25 connector. The complement to this port is the DTE-only port using a male DB-25 connector, as shown in Figure 2.

If the port must accommodate both DTE and DCE modes, the mapping of the drivers and receivers to connector pins must change accordingly. For example, in Figure 1, driver 1 in the LTC1543 is connected to pin 3 and pin 16 of the DB-25 connector. In DTE mode, as shown in Figure 2, driver 1 is mapped to pins 2 and 14 of the DB-25 connector. A port that can be configured for either DTE or DCE operation is shown in Figure 3. This configuration requires separate cables for proper signal routing.

Cable-Selectable Multiprotocol Interface

The interface protocol may be selected by simply plugging the appropriate interface cable into the connector. A cable-selectable multiprotocol DTE/DCE interface is shown in Figure 4.

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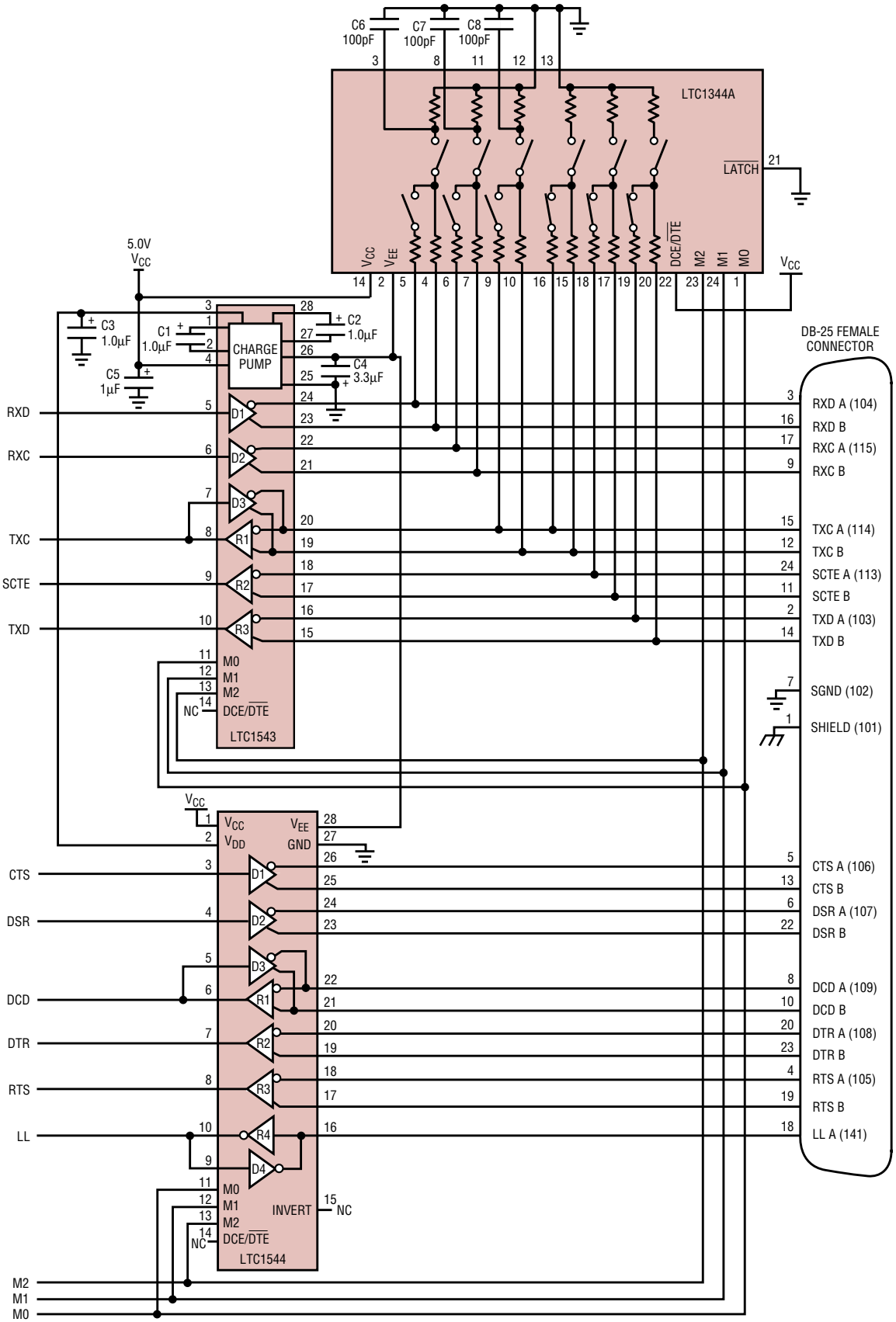

Figure 1. Controller-selectable DCE port with DB-25 connector

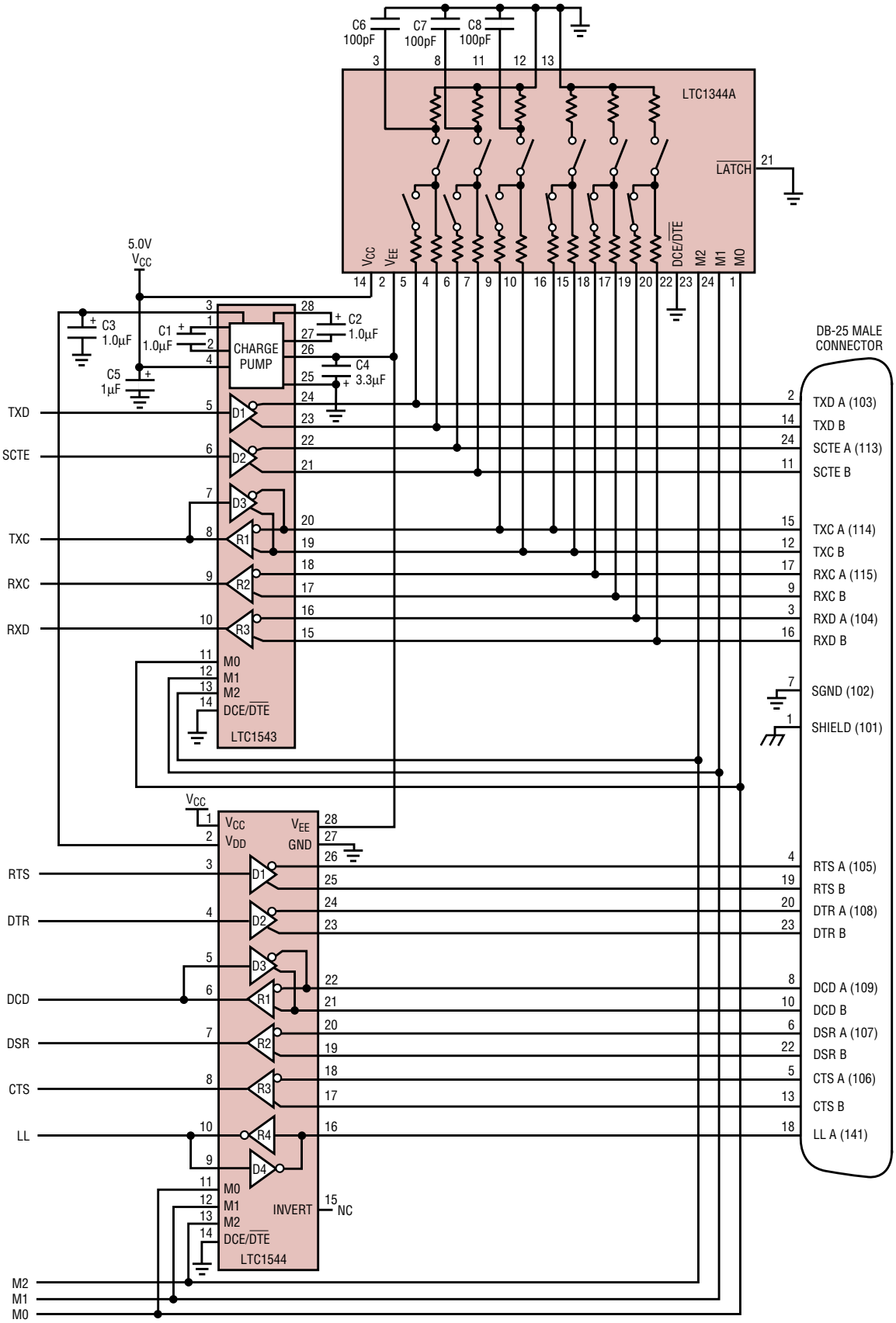

Figure 2. Controller-selectable multiprotocol DTE port with DB-25 connector

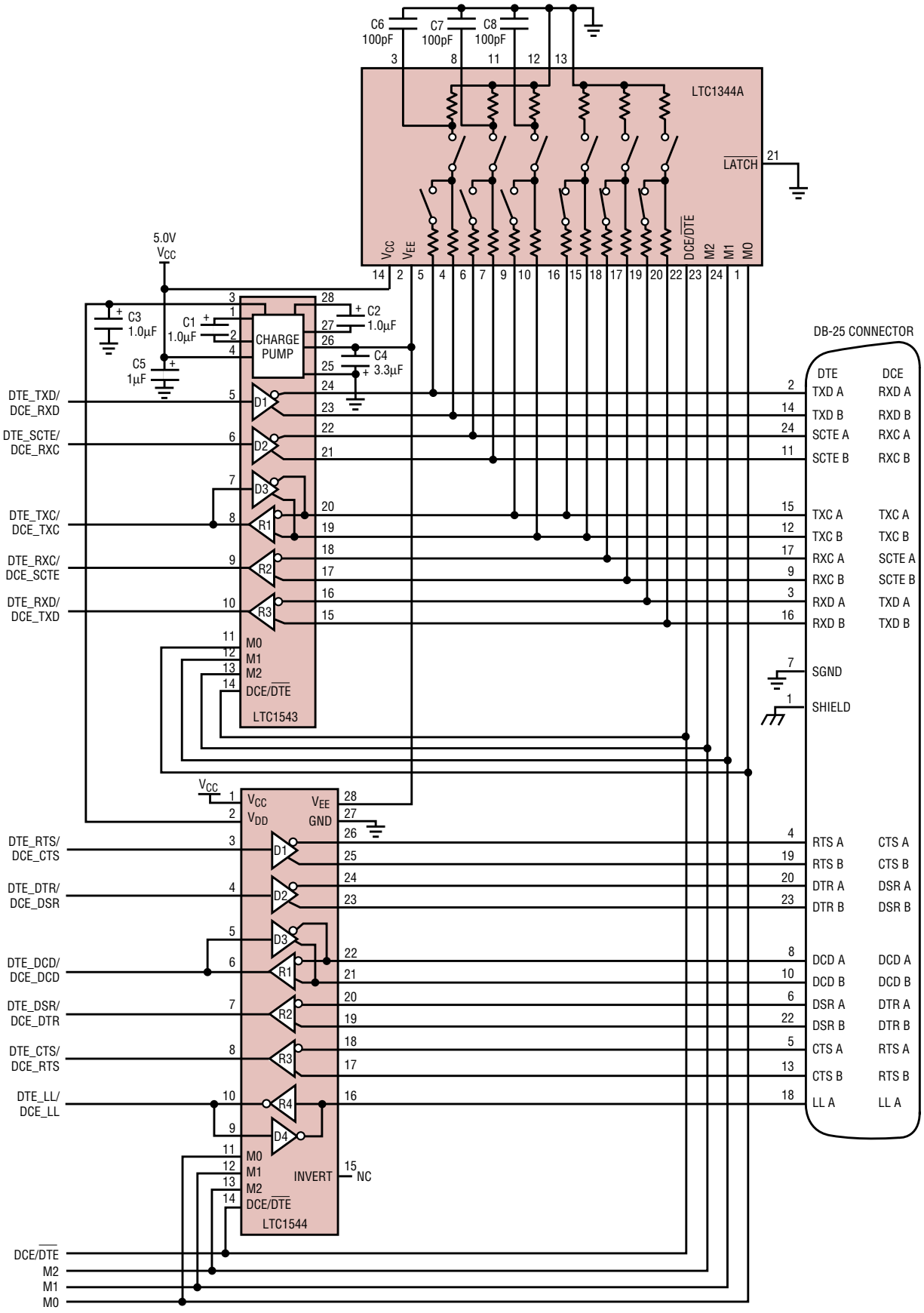

Figure 3. Controller-selectable DTE/DCE port with DB-25 connector

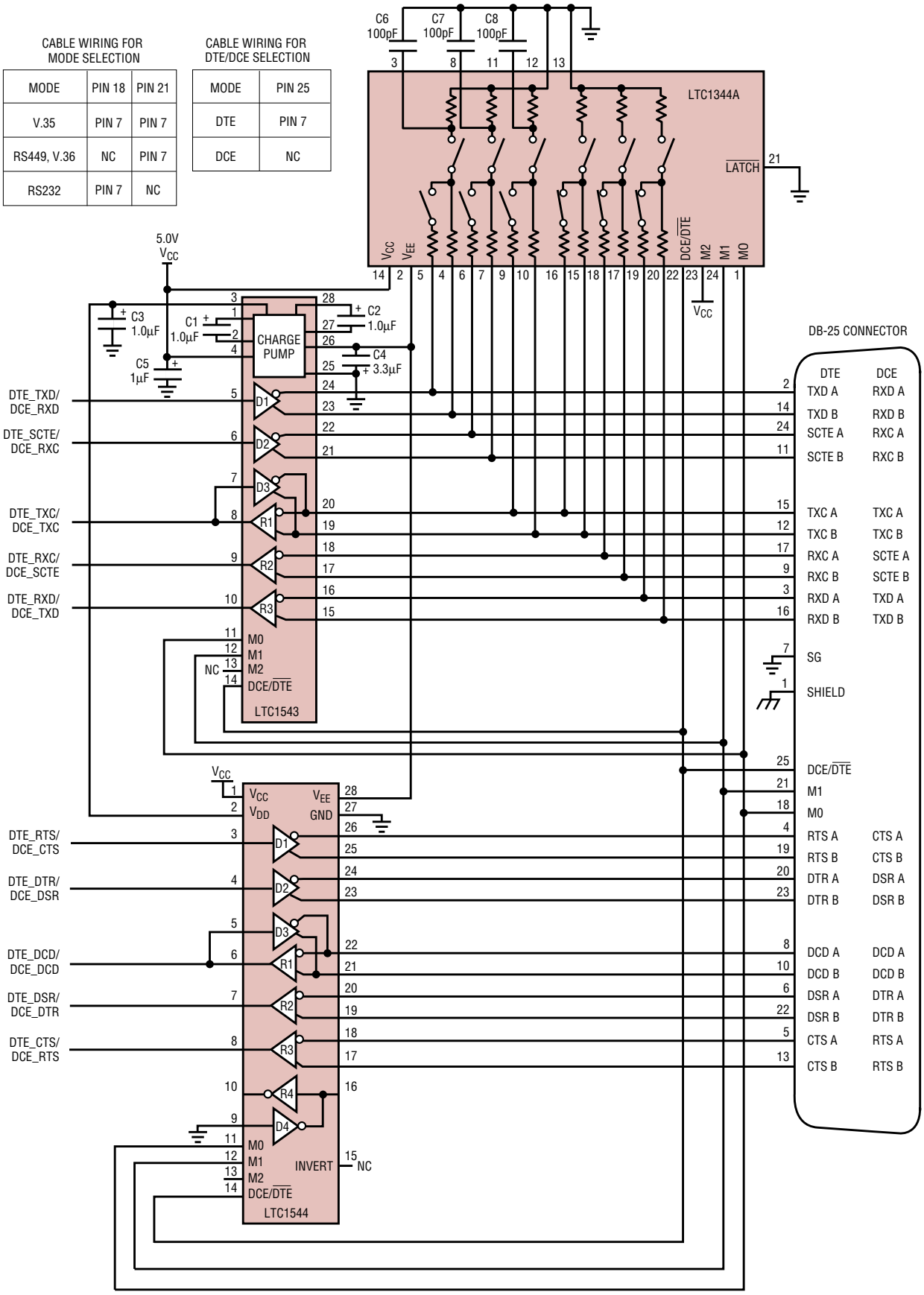

Figure 4. Cable-selectable multiprotocol DTE/DCE port

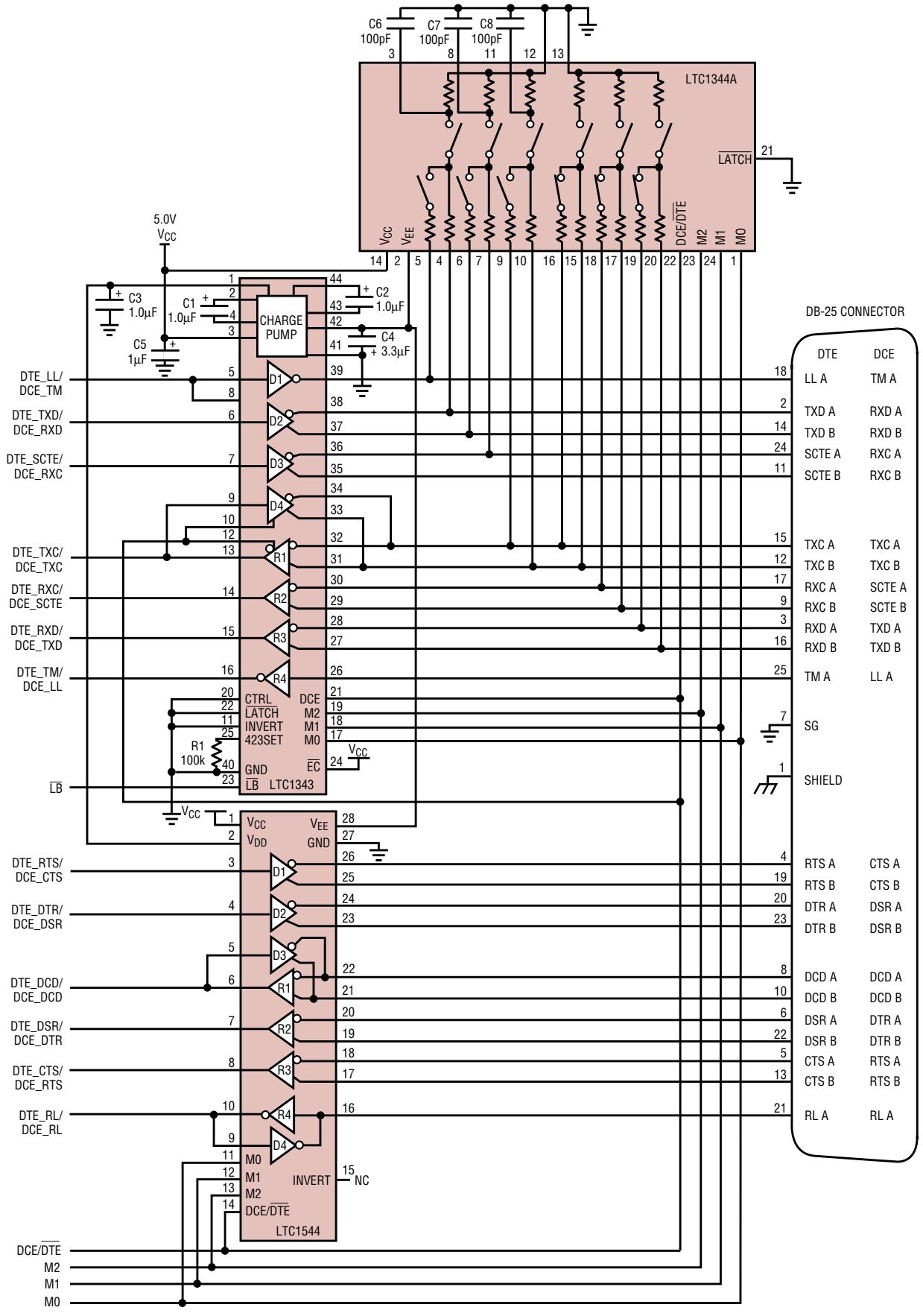

Figure 5. Controller-selectable multiprotocol DTE/DCE port with RLL, LL, TM and DB-25 connector

High Clock-to-Center Frequency Ratio LTC1068-200 Extends Capabilities of Switched Capacitor Highpass Filter

by Frank Cox

The circuit in Figure 1 is a 1kHz 8th order Butterworth highpass filter built with the LTC1068-200, a switched capacitor filter (SCF) building block. In the past, commercially available switched capacitor filters have had limited use as highpass filters because of their sampled-data nature. Sampled-data systems generate spurious frequencies when the sampling clock of the filter and the input signal mix. These spurious frequencies can include sums and differences of the clock and the input, in addition to sums and differences of their harmonics. The input of the filter must be band limited to remove frequencies that will mix with the clock and end up in the passband of the filter. Unfortunately, the passband of a highpass filter extends upward in frequency by its very nature. If you have to band limit the input signal too much you will also limit the passband of the filter, and hence its usefulness.

What makes this filter different is the 200:1 clock-to-center frequency ratio (CCFR) and the internal sampling scheme of the LTC1068-200. Figure 2a shows the amplitude response of the filter plotted against frequency from 100Hz to 10kHz. For comparison, Figure 2b shows the same filter built with an LTC1068-25. This is a 25:1 CCFR part. The 200:1 CCFR filter delivers almost 30dB more ultimate attenuation in the stopband. A standard amplitude vs frequency plot of a highpass filter can be misleading because it masks some of the aforementioned spurious signals introduced into the passband. Figure 3a is a spectrum plot of the 200:1 filter with a single 10kHz tone on the input. This plot shows that the

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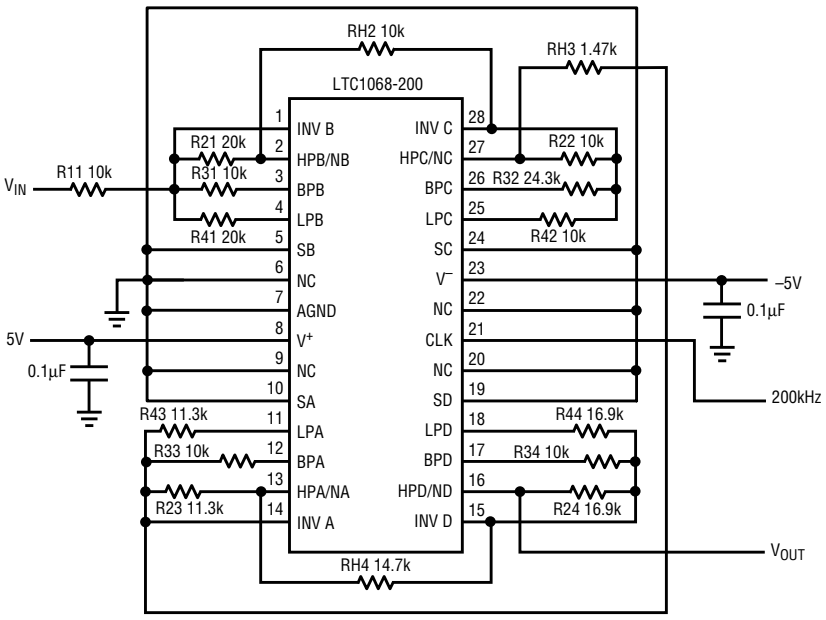


Figure 1. LTC1068-200 1kHz 8th order Butterworth highpass filter

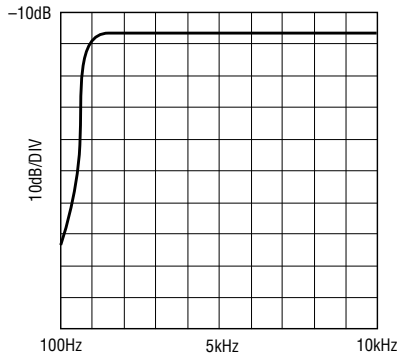


Figure 2a. Amplitude vs frequency response of Figure 1's circuit

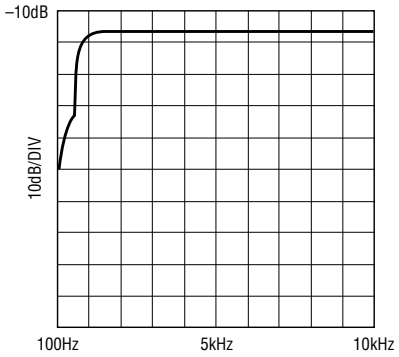


Figure 2b. Amplitude vs frequency response of comparable filter using the LTC1068-25

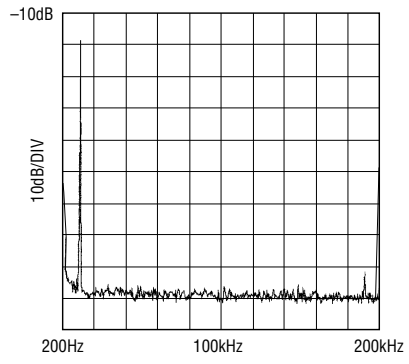


Figure 3a. Spectrum plot of Figure 1's circuit with a single 10kHz input

LT1533 Ultralow Noise Switching Regulator for High Voltage or High Current Applications

by Jim Williams

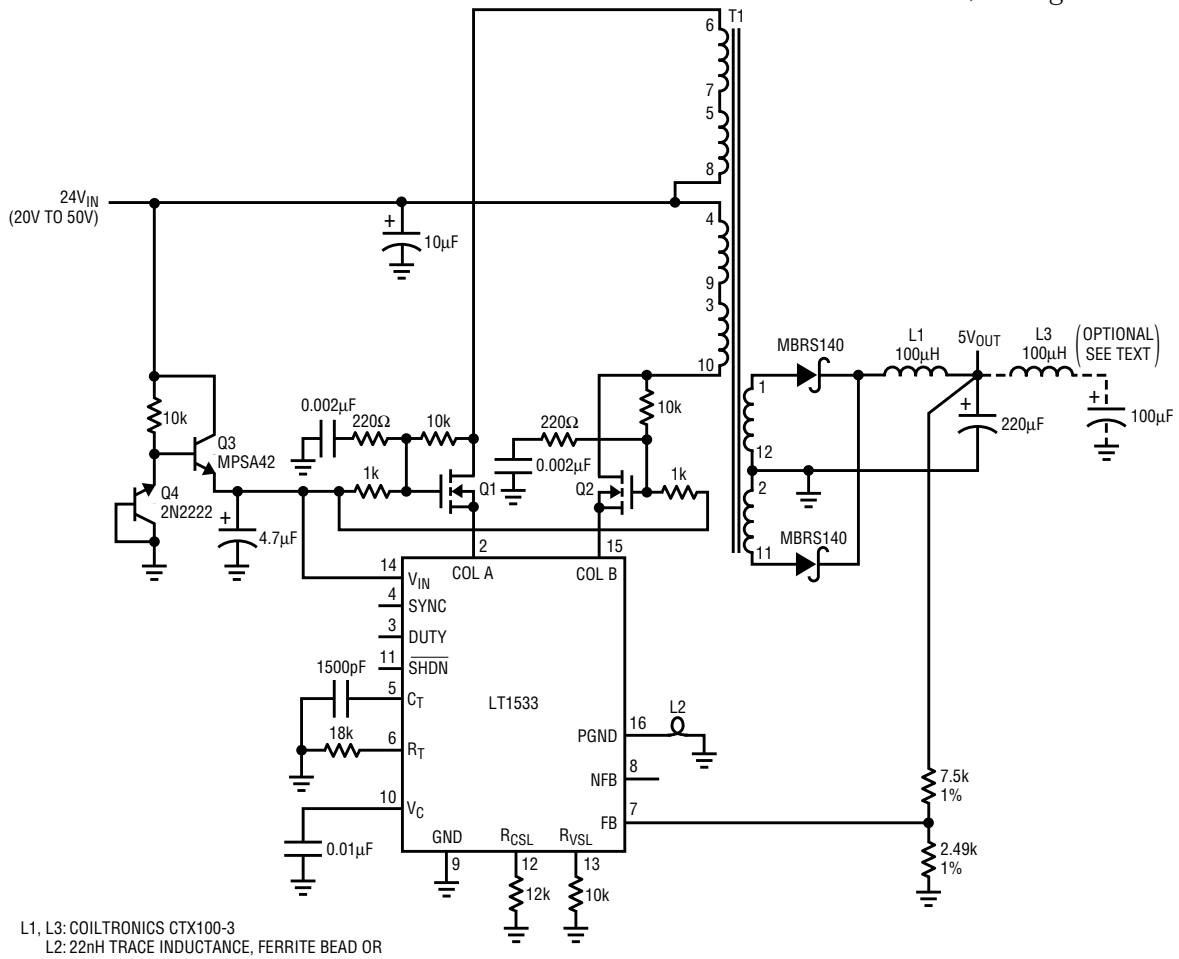
The LT1533 switching regulator[1, 2] achieves 100µV output noise by using closed-loop control around its output switches to tightly control switching transition time. Slowing down switch transitions eliminates high frequency harmonics, greatly reducing conducted and radiated noise.

The part's 30V, 1A output transistors limit available power. It is possible to exceed these limits while maintaining low noise performance by using suitably designed output stages.

High Voltage Input Regulator

The LT1533's IC process limits collector breakdown to 30V. A complicating factor is that the transformer causes the collectors to swing to twice the supply voltage. Thus, 15V represents the maximum allowable input supply. Many applications require higher voltage inputs; the circuit in Figure 1 uses a cascoded[3] output stage to achieve such high voltage capability. This 24V to 5V (V_{IN} = 20V–50V) converter is reminiscent of previous LT1533 circuits, except for the presence of Q1 and Q2.[4] These devices, interposed between the IC and the transformer, constitute a cascoded high voltage stage. They provide voltage gain while isolating the IC from their large drain voltage swings.

Normally, high voltage cascodes are designed to simply supply voltage isolation. Cascoding the LT1533 presents special considerations because the transformer's instantaneous voltage and current information must be accurately transmitted, albeit at lower amplitude, to the LT1533. If this is not done, the regulator's slew-control



L1, L3: COILTRONICS CTX100-3
L2: 22nH TRACE INDUCTANCE, FERRITE BEAD OR INDUCTOR COILCRAFT B-07T TYPICAL
Q1, Q2: MTD6N15
T1: COILTRONICS VP4-0860

Figure 1. A low noise 24V to 5V converter (V_{IN} = 20V–50V): cascoded MOSFETs withstand 100V transformer swings, permitting the LT1533 to control 5V/2A output.

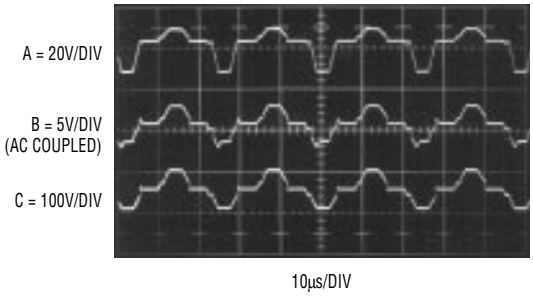


Figure 2. MOSFET-based cascode permits the regulator to control 100V transformer swings while maintaining a low noise 5V output. Trace A is Q1's source, Trace B is Q1's gate and Trace C is the drain. Waveform fidelity through cascode permits proper slew-control operation.

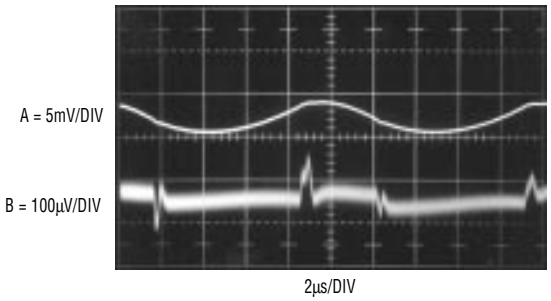


Figure 4. Waveforms for Figure 3 at 10W output: Trace A shows fundamental ripple with higher frequency residue just discernible. The optional LC section results in Trace B's 180µV_{P-P} wideband noise performance.

loops will not function, causing a dramatic output noise increase. The AC-compensated resistor dividers associated with the Q1–Q2 gate-drain biasing serve this purpose, preventing transformer swings coupled via gate-channel capacitance from corrupting the cascode's waveform-transfer fidelity. Q3 and associated components provide a stable DC termination for the dividers while protecting the LT1533 from the high voltage input.

Figure 2 shows that the resultant cascode response is faithful, even with 100V swings. Trace A is Q1's source; traces B and C are its gate and drain, respectively. Under these conditions, at 2A output, noise is inside 400µV peak.

Current Boosting

Figure 3 boosts the regulator's 1A output capability to over 5A. It does this with simple emitter followers (Q1–Q2). Theoretically, the followers preserve T1's voltage and current waveform information, permitting the LT1533's slew-control circuitry to function. In practice, the transistors must be relatively low beta types. At 3A collector current, their beta of 20 sources ≈150mA via the Q1–Q2 base paths, adequate for proper slew-loop operation.[5] The follower loss limits efficiency to about 68%. Higher input voltages minimize follower-induced loss, permitting efficiencies in the low 70% range.

Figure 4 shows noise performance. Ripple measures 4mV (Trace A) using a single LC section, with high frequency content just discernible. Adding the optional second LC section reduces ripple to below 100µV (trace B), and high frequency content is seen to be inside 180µV (note ×50 vertical scale-factor change).

Notes:

1 Witt, Jeff. The LT1533 Heralds a New Class of Low Noise Switching Regulators. *Linear Technology* VII:3 (August 1997).

2 Williams, Jim. *LTC Application Note 70: A Monolithic Switching Regulator with 100µV Output Noise*. October 1997.

3 The term "cascode," derived from "cascade to cathode," is applied to a configuration that places active devices in series. The benefit may be higher breakdown voltage, decreased input capacitance, bandwidth improvement or the like. Cascoding has been employed in op amps, power supplies, oscilloscopes and other areas to obtain performance enhancement.

4 This circuit derives from a design by Jeff Witt of Linear Technology Corp.

5 Operating the slew loops from follower base current was suggested by Bob Dobkin of Linear Technology Corp.

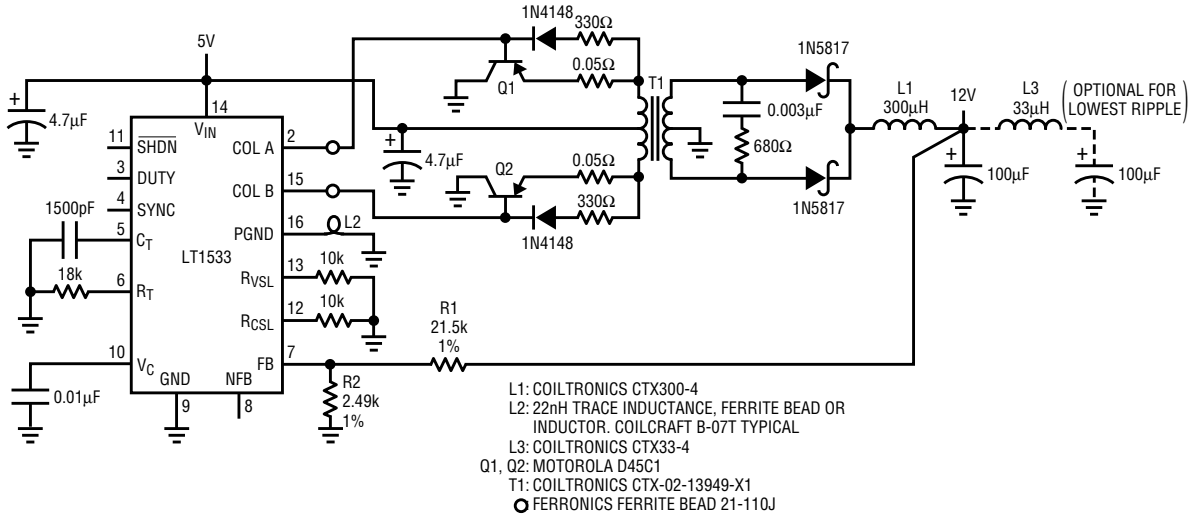


Figure 3. A 10W low noise 5V to 12V converter: Q1–Q2 provide 5A output capacity while preserving the LT1533's voltage/current slew control. Efficiency is 68%. Higher input voltages minimize follower loss, boosting efficiency above 71%.

A Complete Battery Backup Solution Using a Rechargeable NiCd Cell

by L.Y. Lin and S.H. Lim

Battery-powered systems, including notebook computers, personal digital assistants (PDAs) and portable instruments, require backup systems to keep the memory alive while the main battery is being replaced. The most common solution is to use an expensive, nonrechargeable lithium battery. This solution requires low-battery detection, necessitates battery access and invites inadvertent battery removal. The LTC1558 battery backup controller eliminates these problems by permitting the use of a single, low cost 1.2V rechargeable Nickel-Cadmium (NiCd) cell. The LTC1558 has a built-in fast-/trickle-mode charger that charges the NiCd cell when main power is present.

Figure 1 shows a typical application circuit with an LTC1558-3.3 providing backup power to an LTC1435 synchronous step-down switching regulator. The backup circuit components consist of the NiCd cell, R11–R14, C11–C12, L11 and Q11. SW11 and R15 provide a soft or hard reset function.

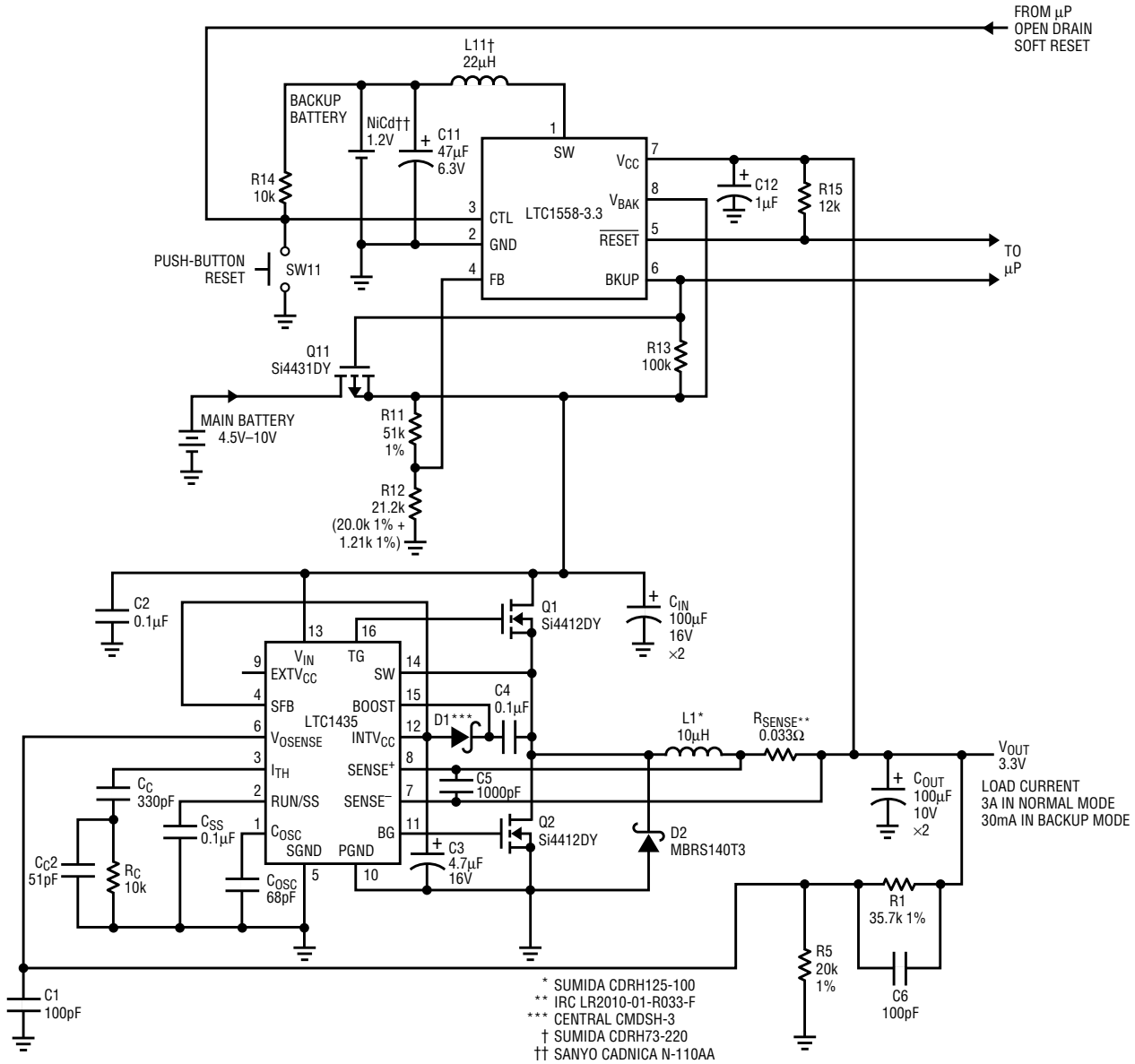


Figure 1. LTC1558 backup system with LTC1435 as main system regulator

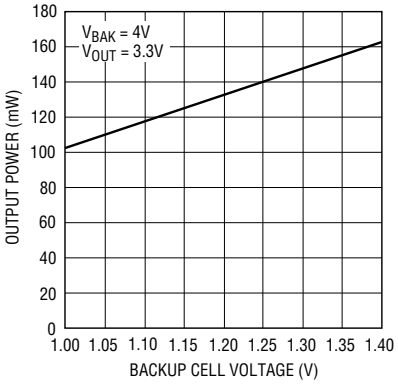


Figure 2. 3.3V output power vs backup cell voltage

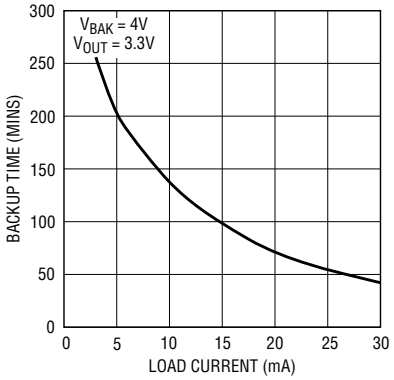


Figure 3. Backup time vs 3.3V output load current

Normal Mode (Operation from the Main Battery)

During normal operation, the LTC1435 is powered from the main battery, which can range from 4.5V to 10V (for example, a 2-series or 2-series × 2-parallel Li-Ion battery pack, or the like) and generates the 3.3V system output. The LTC1558 operates in standby mode. In standby mode, the LTC1558 BKUP (backup) pin is pulled low and P-channel MOSFET Q11 is on. The NiCd cell is fast charged by a 15mA current source connected between the LTC1558's V_{CC} and SW pins. Once the NiCd cell is fully charged (according to the LTC1558's gas-gauge counter), the LTC1558 trickle charges the NiCd cell. R14 sets the trickle-charge current according to the formula $I_{(TRICKLE)} = 10 \bullet (V_{NiCd} - 0.5)/R14$. The trickle-charge current is set to overcome the NiCd cell's self-discharge current, thereby maintaining the cell's full charge.

Backup Mode (Operation from the Backup Battery)

The main battery voltage is scaled down through resistor divider R11–R12 and monitored by the LTC1558 via the FB pin. If the voltage on the FB pin drops 7.5% below the internal 1.272V reference voltage (due to discharging or exchanging the main battery), the system enters backup mode. In backup mode, the LTC1558's internal switches and L11 form a synchronous boost converter that generates a regulated 4V at V_{BAK}. The LTC1435 operates from this supply voltage to generate the 3.3V output voltage. The BKUP pin is pulled high by R13 and Q11 turns off , leaving its body diode reverse biased. The BKUP pin also alerts the system microprocessor. C11, a 47µF capacitor, provides a low impedance bypass to handle the boost converter's transient load current; otherwise, the voltage drop across the NiCd cell's internal resistance would activate the LTC1558's undervoltage-lockout function. Table 1 shows several values of V_{FB} vs the V_{BAK} voltage. Figure 2 shows the maximum output power available at the 3.3V output vs the NiCd cell voltage. Over 100mW of output power is achieved for a NiCd cell voltage greater than 1V. Figure 3 shows the backup time vs the 3.3V load current using a Sanyo Cadnica N-110AA cell (standard series with a capacity of 110mAhrs). Over one hour of backup time is realized for less than 80mW of 3.3V output power.

Battery-powered systems, including notebook computers, personal digital assistants (PDAs) and portable instruments, require backup systems to keep the memory alive while the main battery is being replaced. The most common solution is to use an expensive, nonrechargeable lithium battery.

Table 1. V_{FB} and V_{BAK} voltages

Relative % Below V_{REF}	% of V_{REF}	V_{FB}	V_{BAK}
–0%	100%	1.272V	4.332V
–6%	94%	1.196V	4.073V
–7.5%	92.5%	1.177V	4.008V

Recovery from Backup Mode to Normal Mode

When a new main battery pack is inserted into the system, Q11's body diode forward biases. Once the voltage at the FB pin increases to more than 6% below V_{REF}, the boost converter is disabled and the system returns to normal mode. The BKUP pin pulls low and turns Q11 back on. This allows the new battery pack to supply input power to the LTC1435. The LTC1558 now accurately replenishes the amount of charge removed from the NiCd cell through the internal charger and gas-gauge counter.

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Zero-Bias Detector Yields High Sensitivity with Nanopower Consumption

by Mitchell Lee

RF ID tags, circuits that detect a "wake-up" call and return a burst of data, must operate on very low quiescent current for months or years, yet have enough battery power in reserve to answer an incoming call. For smallest size, most operate in the ultrahigh frequency range, where the design of a micropower receiver circuit is problematic. Familiar techniques, such as direct conversion, super regeneration or superhetrodyne, consume far too much supply current for long battery life. A better method involves a technique borrowed from simple field-strength meters: a tuned circuit and a diode detector.

Figure 1 shows the complete circuit, which was tested for proof-of-concept at 445MHz. This circuit contains a couple of improvements over the standard L/C-with-whip field-strength meter. Tuned circuits aren't easily constructed or controlled at UHF, so a transmission line is used to match the detector diode (1N5712) to a quarter-wave whip antenna. The 0.23λ transmission-line section transforms the 1pF (350Ω) diode junction capacitance to a virtual short at the base of the antenna. At the same time, it converts the received antenna current to a voltage loop at the diode, giving excellent sensitivity.

Biasing the detector diode can improve sensitivity,[1] but only when the diode is loaded by an external DC resistance. Careful curve-tracer examination of the 1N5712 at the origin reveals that it follows the ideal diode equation, with scales of millivolts and nanoamperes. To use a zero-bias diode at the origin, the external comparator circuitry must not load the rectified output.

The LTC1540 nanopower comparator and reference is a good choice for this application because it not only presents no load to the diode, but also draws only 300nA from the battery. This represents a 10-times improvement in battery life over biased detector schemes.[2] The input is CMOS, and input bias current consists of leakage in a small ESD-protection cell connected between the input and ground. The input leakage measures in the picoampere range, whereas the 1N5712 leaks hundreds of picoamperes. Any rectified output from the diode is loaded by the diode itself, not by the LTC1540, and the sensitivity can match that of a loaded, biased detector.

The rectified output is monitored by the LTC1540 comparator. The LTC1540's internal reference is used to set up a threshold of about 18mV at the inverting input. A rising edge at the comparator output triggers a one-shot, which temporarily enables answer-back and any other pulsed functions.

Total supply current is 400nA, consuming just 7mAH battery life over a period of five years. Monolithic one-shots draw significant load current, but the '4047 is about the best in this respect. A one-shot constructed from discrete NAND gates draws negligible power.

Sensitivity is excellent, and the circuit can detect about 200mW from a reference dipole at 100 feet. Range, of course, depends on operating frequency, antenna orientation and surrounding obstacles. Sensitivity is independent of supply voltage; this receiver will work just as well with a 9V battery as with a single lithium cell.

The length of the transmission line does not scale with frequency. Owing to a decrease in diode reactance, the electrical length will shorten as frequency increases. Adjust the line length for minimum feed-point impedance at the operating frequency. If an impedance analyzer is used to measure the line, a 1pF capacitor can be substituted for the diode to avoid large signal effects in the diode itself. Consult the manufacturer's data sheet for accurate characterization of diode impedance at the frequency of interest.

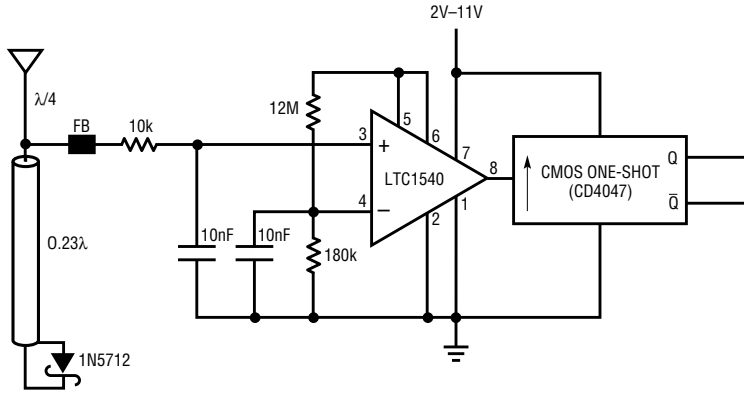

Figure 1. Nanopower field detector

Notes:

1. Eccles, W.H. Wireless Telegraphy and Telephony, Second Edition. Ben Brothers Limited, London, 1918, page 272.
2. Lee, Mitchell. "Biased Detector Yields High Sensitivity with Ultralow Power Consumption." *Linear Technology* VII:1(February 1997), page 21.

Micropower Octal 10-Bit DAC Conserves Board Space with SO-8 Footprint

by Kevin R. Hoskins

Introduction

Historically, many circuits have relied on potentiometers for adjustment or control. Increasingly, microcontrollers and microprocessors are finding applications in these circuits. The inclusion of processors can eliminate potentiometers, replacing them with digital-to-analog converters (DACs). Fulfilling this need is the LTC1660.

Features

Eight DACs in 0.045in^2

The LTC1660 is the latest multichannel DAC from Linear Technology. This 10-bit, voltage-output, octal DAC is designed to conserve board space. Packaged in a 16-pin narrow SSOP, it has an 8-pin SO footprint. Figure 1 is a block diagram showing the LTC1660's major circuit features.

Inherent 10-Bit Monotonicity and Linearity (DNL) Performance

The LTC1660 uses a DAC architecture that features excellent ±0.5dB differential linearity accuracy, ensuring inherently monotonic performance. This is important for closed-loop control applications, since nonmonotonic operation compromises loop stability. Figures 2a and 2b show the LTC1660's INL and DNL performance, respectively.

Reference Input

The LTC1660 uses a single external reference voltage for all its internal DACs. This voltage sets its full-scale output range. The reference voltage magnitude has a range of 0V to V_{CC}. Figure 3 shows a micropower LT1460-2.5 voltage reference setting the LTC1660's full-scale output to 2.5V.

Rail-to-Rail Output Amplifiers

Each internal DAC has an amplifier that buffers its output. The amplifiers' output voltage can swing rail-to-rail; they can source or sink up to 5mA while maintaining guaranteed linearity and monotonicity performance. Additionally, the amplifiers can easily drive 1000pF and remain stable. Higher capacitive loads (such as 0.1µF) can be driven by placing a small value resistor (100Ω typical) in series with the output pin.

Single Supply, 60µA per DAC

The LTC1660 maintains its specified operation over the wide supply range of 2.7V to 5.5V. To ensure efficient operation on this supply range, the total typical supply current drawn is just 480µA. The wide supply range and low current requirements make this DAC ideal for battery-powered applications.

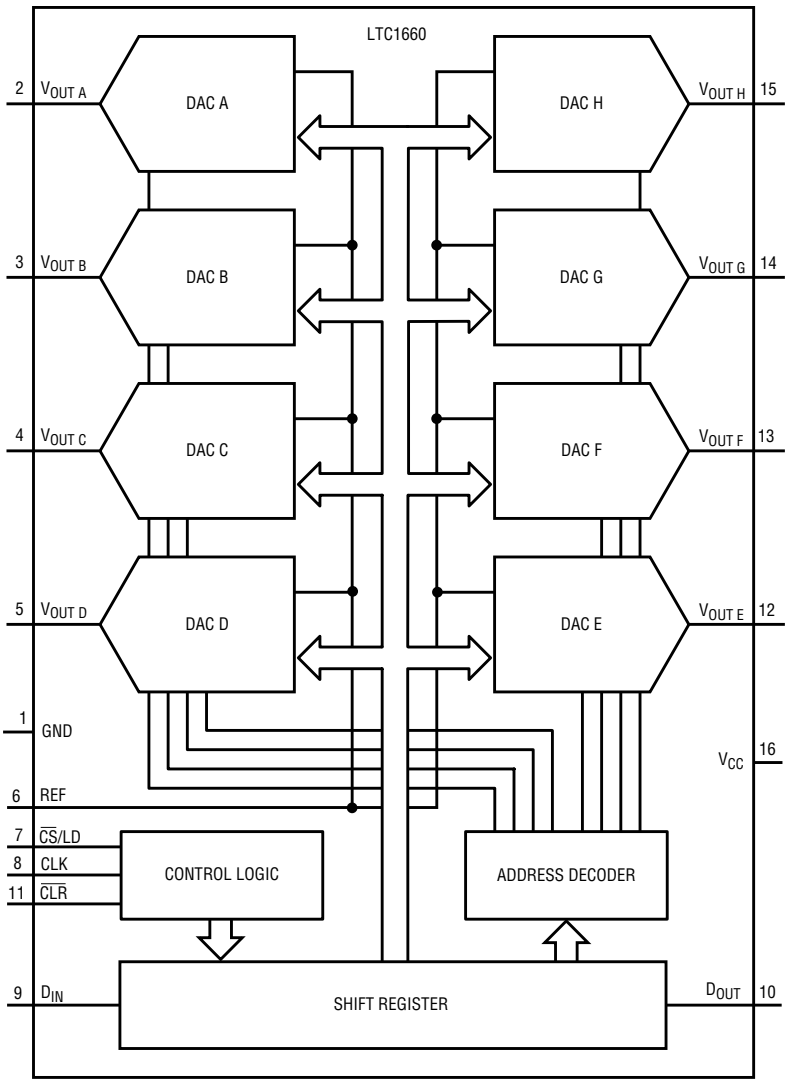

Figure 1. LTC1660 block diagram

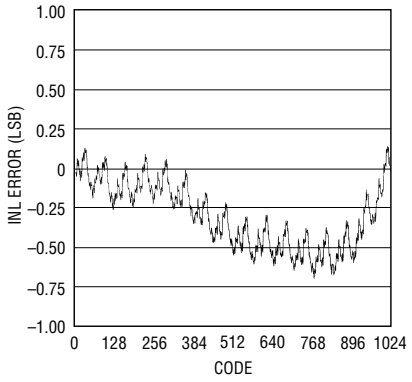

Figure 2a. LTC1660 integral nonlinearity error

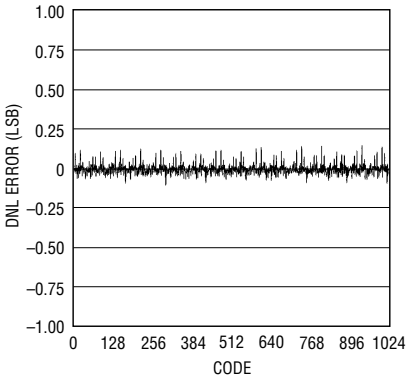

Figure 2b. LTC1660 differential nonlinearity error

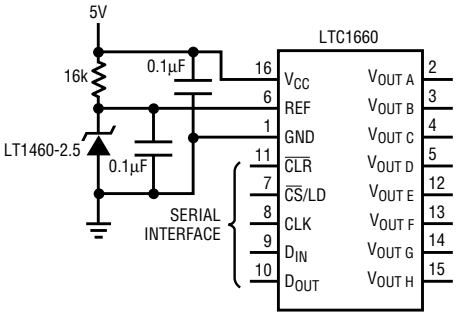

Figure 3. An LT1460 2.5V reference sets the LTC1660's full-scale output to 2.5V.

SLEEP Mode

Further power saving is possible when the LTC1660 is placed in SLEEP mode. Activating SLEEP mode shuts off all internal bias currents and places the output amplifiers in a high impedance state. The SLEEP mode reduces current consumption to 1µA or less. The digital circuitry remains active, retaining the stored values for each DAC. There are two ways to take the part out of SLEEP mode: loading any ADDRESS/CONTROL value other than SLEEP mode or applying a logic low to the $\overline{CLR}$ pin. The last technique awakens the LTC1660 and sets all eight outputs to 0V.

Serial Interface

The eight internal DACs are addressed individually over a 3-wire, SPI-compatible interface. The three signals are Chip Select/Load ($\overline{CS}$/LD), Serial Clock (CLK) and Data In (D_{IN}).

Schmitt Trigger Inputs

The LTC1660's Schmitt trigger digital inputs prevent false triggers when responding to noisy signals or those having slow rise or fall times. This quality makes the LTC1660 ideal for remote placement at the end of long serial transmission lines or lines that use optoisolators.

D_{OUT} Daisy Chain

Another feature of the LTC1660's serial interface is its D_{OUT} pin. The current contents of the internal shift register are shifted out on this pin as new data is shifted in on the D_{IN} pin. This pin makes it possible to connect multiple LTC1660s and other LTC DACs to the same serial data line. The daisy chain is linked by connecting a part's D_{OUT} pin to the D_{IN} pin of the next part in the chain. The advantages of the single serial data line include reduced circuit board space, reduced radiation that results from fewer circuit traces and conservation of limited microcontroller or microprocessor I/O lines.

Power-On Reset

The LTC1660's power-on reset ensures that the output voltage on each DAC is set to 0V when power (2.7V–5.5V) is first applied to the V_{CC} pin.

Asynchronous CLEAR

This active low input will asynchronously reset all eight DAC outputs to 0V when a logic low is applied to this pin. It also deactivates the SLEEP mode.

Applications

The LTC1660 shines brightly in applications that take advantage of its micropower, linearity and versatility. The applications include offset and gain adjust in industrial control systems and AGC and transmit power adjustment in wireless communication.

continued on page 33

Table 1. DAC address/control functions

Address/Control				Action
Bit_{14}	Bit_{13}	Bit_{12}	Bit_{11}	
0	0	0	0	No Update
0	0	0	1	Load DAC A
0	0	1	0	Load DAC B
0	0	1	1	Load DAC C
0	1	0	0	Load DAC D
0	1	0	1	Load DAC E
0	1	1	0	Load DAC F
0	1	1	1	Load DAC G
1	0	0	0	Load DAC H
1	0	0	1	None
1	0	1	0	None
1	0	1	1	None
1	1	0	0	None
1	1	0	1	None
1	1	1	0	SLEEP Mode
1	1	1	1	Load all DACSs with the same 10-bit code

Tiny MSOP Dual Switch Driver is SMBus Controlled

by Peter Guan

Introduction

The LTC1623 SMBus™ switch controller offers an inexpensive, space-saving alternative for controlling peripherals in today's complex portable computer systems. Pin-to-pin connections between the system controller and each peripheral device not only result in complicated wiring, but also limit the number and type of peripheral devices connected to the system controller. Using the SMBus architecture, the LTC1623 eliminates these problems by requiring only two bus wires and allowing easy upgrades and additions of new peripherals.

The SMBus

The SMBus is a low power serial bus developed by Intel and Duracell. Only two bus lines, DATA and CLK, are needed to establish a set of protocols for communication between the bus master and slaves. Using the SEND BYTE protocol of the SMBus to receive and execute commands from the bus master, each LTC1623 controls the operation of two independent external switches. To identify itself on the SMBus, the LTC1623 has two three-state address pins. In other words, up to eight LTC1623s can be programmed to control up to sixteen different switches.

LTC1623 Design Information

A timing diagram of the SEND BYTE protocol is shown in Figure 1. After detecting the Start signal from the bus master (a high-to-low transition on the DATA line while CLK is high), the LTC1623 shifts in the address byte, which consists of seven address bits and one read/write bit. If the address byte matches, the LTC1623 acknowledges the master and then shifts in the command byte whose two LSBs are the controlling signals for the two external switches. Afterwards, the LTC1623 again acknowledges the master so that the master can terminate the transaction by sending a Stop signal (a DATA transition from low to high while CLK is high).

The LTC1623 adheres strictly to the SMBus specification of 0.6V V_{IL} and 1.4V V_{IH} over the entire operating range of 2.7V to 5.5V. The two built-in charge pump triplers with micropower feedback networks guarantee full enhancement of the two external logic-level MOSFET switches without excess gate overdrive. The output gate-drive voltage is regulated to a maximum of 6V above V_{IN}.

Applications

The main application of the LTC1623 is to control two external high-side N-channel switches (Figure 2). As seen in the figure, a 0.1µF capacitor and a 1k resistor are placed on each gate-drive output to respectively slow down the turn-on time of the external switch and to eliminate any oscillations caused by the parasitic capacitance of the external switch and the parasitic inductance of the connecting wires.

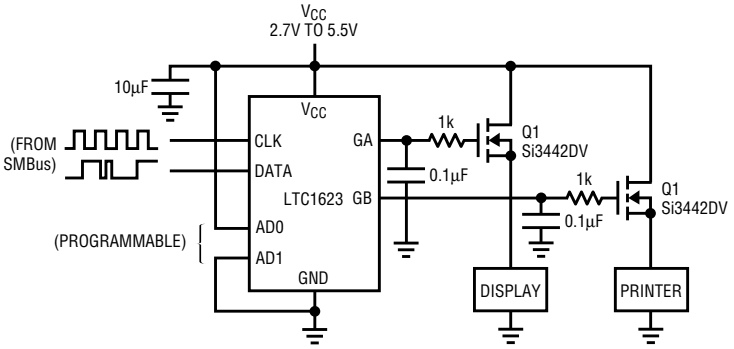

Figure 2. LTC1623 controlling two high-side switches

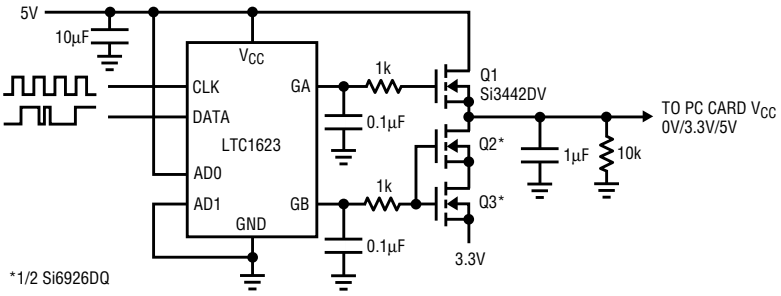

Figure 3. PC Card 3.3V/5V switch matrix.

SMBus is a trademark of Intel Corp.

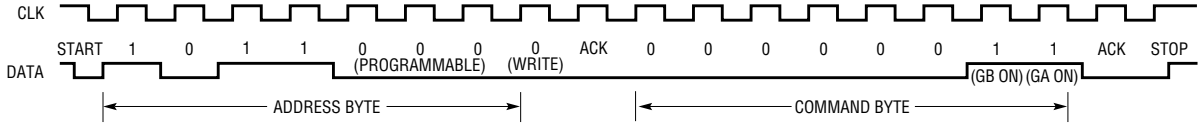

Figure 1. SMBus SEND BYTE protocol timing diagram

Tracking the growing popularity of portable communication systems, the LTC1623 makes a very handy single-slot 3.3V/5V PC Card switch matrix. As shown in Figure 3, this circuit enables a system controller to switch either a 3.3V or a 5V supply to any of its SMBus-addressed peripherals. Besides N-channel switches, the LTC1623 can also be used to control a P-channel switch, as shown in Figure 4. As a result, the load connected to the P-channel switch will be turned on upon power-up of the LTC1623, whereas the other load must wait for a valid address and command to be powered.

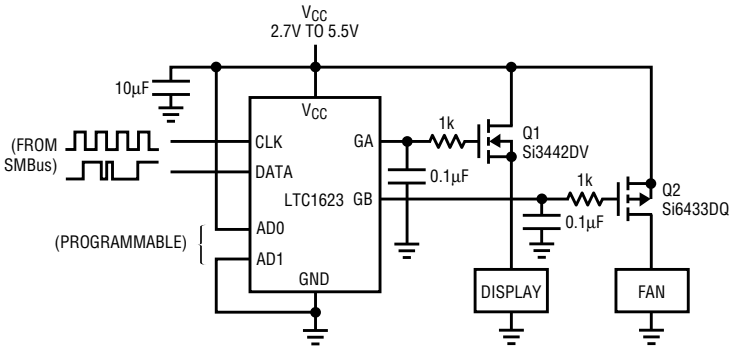

Figure 4. LTC1623 controlling a P-channel switch (Q2)

Conclusion

With a standby current of only 17µA and a tiny 8-lead MSOP (or SO) footprint, the LTC1623 offers a simple and efficient solution for managing system peripherals using the SMBus architecture.

LTC1543, continued from page 17

The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable. The internal pull-up current sources ensure a binary 1 when a pin is left unconnected and also ensure that the LTC1543/LTC1544/LTC1344A enter the no-cable mode when the cable is removed. In the no-cable mode, the LTC1543/LTC1544 power supply current drops to less than 200µA and all of the LTC1543/LTC1544 driver outputs will be forced into the high impedance state.

Adding Optional Test Signal

In some cases, the optional test signals local loopback (LL), remote loopback (RL) and test mode (TM) are required but there are not enough drivers and receivers available in the LTC1543/LTC1544 to handle these extra signals. The solution is to combine the LTC1544 with the LTC1343. By using the LTC1343 to handle the clock and data signals, the chip set gains one extra single-ended driver/receiver pair. This configuration is shown in Figure 5.

Compliance Testing

A European standard EN 45001 test report is available for the LTC1543/LTC1544/LTC1344A chip set. The report provides documentation on the compliance of the chip set to Layer 1 of the NET1 and NET2 standard. A copy of this test report is available from LTC or from Detecon, Inc. at 1175 Old Highway 8, St. Paul, MN 55112.

Conclusion

In the world of network equipment, the product differentiation is mostly in the software and not in the serial interface. The LTC1543, LTC1544 and LTC1344A provide a simple yet comprehensive solution to standards compliance for multiple-protocol serial interface.

Authors can be contacted at (408) 432-1900

LTC1562 continued from page 5

Quadruple 3rd Order 100kHz Butterworth Lowpass Filter

Another example of the flexibility of the virtual-ground inputs is the ability to add an extra, independent real pole by replacing the input resistor in Figure 2 with an R-C-R "T" network. In Figure 10, a 10k input resistor has been split into two parts and the parallel combination of the two forms a 100kHz real pole with the 680pF external capacitor. Four such 3rd order Butterworth lowpass filters can be built from one LTC1562. The same technique can add additional real poles to other filter configurations as well, for example, augmenting Figure 4's circuit to obtain a dual 5th order filter from a single LTC1562.

Conclusion

The LTC1562 is the first truly compact universal active filter, yet it offers instrumentation-grade performance rivaling much larger discrete-component designs. It serves applications in the 10kHz–150kHz range with an SNR as high as 100dB or more (16+ equivalent bits). The LTC1562 is ideal for modems and other communications systems and for DSP antialiasing or reconstruction filtering.

LTC1660 continued from page 30

Accessing the Functionality

Table 1 shows the DAC ADDRESS/CONTROL codes that update each of the DACs, activate the SLEEP mode, cause "No Update", or update all DACs with the same 10-bit value.

The four MSBs (Bit_{15}–Bit_{12}) of the 16-bit data word sent to the LTC1660 select a DAC for updating or a control function such as SLEEP. The next ten bits (Bit_{11}–Bit_2) are the data that sets the selected DAC's output voltage. For example, with a 2.5V reference voltage applied to the LTC1660's pin 6, a value of 819 (1100110011) on Bit_{11}–Bit_2 sets the DAC's output voltage to 819/1024 • 2.5V, = 2.0V. The last two bits (Bit_1–Bit_0) are "don't care." When a 4-bit "no update" code is sent (Bit_{15}–Bit_{12} = 0000 and 1001–1101), the contents of Bit_{11}–Bit_0 are ignored. The SLEEP mode is selected by sending Bit_{15}–Bit_{12} = 1110. The LTC1660 is awakened by applying a logic low to the $\overline{CLR}$ pin or by completing a data load cycle. To awaken the part with a load cycle and return to the same output voltages as before SLEEP, use address/control locations Bit_{15}–Bit_{12} = 0000 or 1001–1101. Using $\overline{CLR}$ to awaken the LTC1660 changes the contents of all DAC registers to zeros and the output voltage to 0V. Finally, all DACs can be forced to the same output voltage by using address/control location Bit_{15}–Bit_{12} = 1111.

Layout, Bypassing and Grounding Considerations

Like all data converters, the LTC1660 performs best when it is properly grounded, bypassed and placed on a PCB layout optimized for low noise. Proper grounding is achieved by placing the part over an analog ground plane. Ideally, no traces should cut through the analog ground plane. If a digital ground plane is present, it should make contact with the analog ground plane at only one point, usually where the board is grounded to the power supply ground. If the board consists of multiple layers, the digital and analog ground planes should not overlap each other. The ground pin (pin 1) should be connected to the analog ground plane.

Two 0.1µF bypass capacitors should be connected between the LTC1660 and the analog ground plane. One capacitor is connected to the V_{CC} input (pin 16) and the other is connected to the reference input (pin 6). Lead lengths should be as short as possible.

To help ensure that digital switching noise does not contaminate the analog output, pins 7–11 should be placed over the digital ground plane and not cross the analog ground plane.

Conclusion

The LTC1660 10-bit octal DAC features a very small narrow SSOP-16 package, micropower operation and power saving SLEEP mode. These features make this the ideal part for dense circuit boards and battery-powered applications.

LTC1068-200 continued from page 23

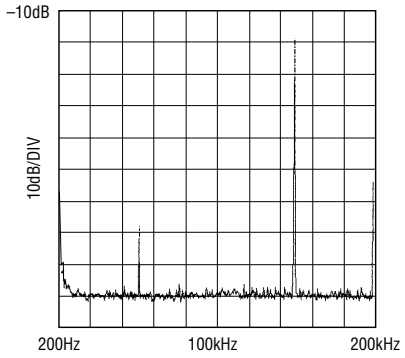

Figure 3b. Spectrum plot of Figure 1's circuit with a single 150kHz input

spurious free dynamic range (SFDR) of the LTC1068 highpass filter is in excess of 70dB. In fact, the filter has a 70dB SFDR for all input signals up to 100kHz. In a 200kHz sampled-data system, you would normally need to band limit the input below 100kHz, the Nyquist frequency. Because the LTC1068 uses double sampling techniques, its useful input frequency range extends to the Nyquist frequency and even above, albeit with some care. Figure 3b shows the LTC1068-200 highpass filter with an input frequency of 150kHz. There is a spurious signal at 50kHz, but even though there is no input filtering, the SFDR is still 60dB. For input signals from 100kHz to 150kHz, the filter demonstrates an SFDR of at least 60dB. The SFDR plot of the same filter built with the LTC1068-25 is shown in Figure 4. Note that the lower CCFR (25:1) part still manages a respectable 55dB SFDR with a 10kHz input. The LTC1068-25 is used primarily for band-limited applications, such as lowpass and bandpass filters.

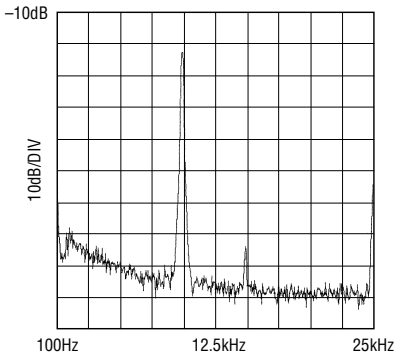

Figure 4. Spectrum plot of a comparable filter using the LTC1068-25 with a single 10kHz input shows a respectable 55dB SFDR.

Note:

The filters for this article were designed using Linear Technology's FilterCAD™ (version 2.0) for Windows®. This program made the design and optimization of these filters fast and easy.

New Device Cameos

Ultralow I_Q LTC1474, LTC1475 Stepdown DC/DC Converter Family Grows

The LTC1474/LTC1475 family has been expanded to cover a complete range of output voltage, package and operating-temperature options. All members of the family feature 3V to 18V (20V Absolute Maximum) operation, 10µA typical quiescent current and programmable peak inductor current. The LTC1474 is controlled by a run pin and features a low-battery comparator that remains active in shutdown. The LTC1475 adds an on/off latch, allowing push-button control of power.

Both the LTC1474 and LTC1475 are available with 3.3V, 5V or adjustable output voltages. All versions are offered in two packages: the industry-standard small outline 8-pin plastic package and the tiny 8-pin MSOP package. MSOP-packaged parts are specified for the commercial temperature range, whereas all LTC1474 S8 versions and the LTC1475 S8 adjustable version are also available specified for the industrial temperature range (see table).

Option	CMS8	CS8	IS8
LTC1474-ADJ	✓	✓	✓
LTC1474-3.3	✓	✓	✓
LTC1474-5	✓	✓	✓
LTC1475-ADJ	✓	✓	✓
LTC1475-3.3	✓	✓	
LTC1475-5	✓	✓	

Every member of the LTC1474/LTC1475 family features operating efficiencies exceeding 90% and a combination of cycle-by-cycle inductor current control and ultralow quiescent current previously unavailable in switching regulators. Strapping two pins together defines a 400mA peak inductor current with no external current sense resistor, allowing up to 300mA output currents. Adding an inexpensive external resistor allows the user to program the peak inductor current to as low as 10mA for efficient low current operation with small inductors.

The LTC1474/LTC1475 are ideal for many quiescent-current-sensitive applications, such as battery-powered, handheld devices, keep-alive power supplies and industrial 4–20mA loops.

LT1534 Ultralow Noise 2A Regulator

The LT1534 is the next in the line of "stealth switchers," DC/DC converters designed to significantly reduce conducted and radiated electromagnetic interference (EMC, EMI). By adjusting the output switch voltage and current slew rates, noise can be reduced to unprecedented levels. These converters can then be used to generate power in applications that previously excluded switchers, including precision instrumentation systems, medical instruments, single-board data acquisition systems and wireless communications. The LT1534 is specifically designed for single-output topologies such as boost, SEPIC and Cuk.

The LT1534 uses a current mode architecture; it includes a single 2A power switch along with all necessary oscillator, control and protection circuitry. Unique error amp circuitry can regulate both positive and negative voltages. The internal oscillator may be synchronized to an external clock. Protection features include cycle-by-cycle short-circuit protection, undervoltage lockout and thermal shutdown. Low shutdown current (12µA typical) and low minimum input voltage requirements (2.7V) make this part suitable for battery-operated applications. The LT1534 is offered in an SO-16 package in a commercial temperature grade.

The user can independently adjust the output switch current slew rate and voltage slew rate. This allows the user to optimally trade off noise and efficiency. Because the slew control reduces the source of switcher noise, it can reduce or eliminate the need for power supply shielding and filtering components.

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

DESIGN TOOLS

Applications on Disk

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp. Available at no charge

SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim. Available at no charge

SwitcherCAD™ — The SwitcherCAD program is a powerful PC software tool that aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. 144 page manual included. $20.00

SwitcherCAD supports the following parts: LT1070 series: LT1070, LT1071, LT1072, LT1074 and LT1076. LT1082. LT1170 series: LT1170, LT1171, LT1172 and LT1176. It also supports: LT1268, LT1269 and LT1507. LT1270 series: LT1270 and LT1271. LT1371 series: LT1371, LT1372, LT1373, LT1375, LT1376 and LT1377.

Micropower SwitcherCAD™ — The MicropowerSCAD program is a powerful tool for designing DC/DC converters based on Linear Technology's micropower switching regulator ICs. Given basic design parameters, MicropowerSCAD selects a circuit topology and offers you a selection of appropriate Linear Technology switching regulator ICs. MicropowerSCAD also performs circuit simulations to select the other components which surround the DC/DC converter. In the case of a battery supply, MicropowerSCAD can perform a battery life simulation. 44 page manual included. $20.00

MicropowerSCAD supports the following LTC micropower DC/DC converters: LT1073, LT1107, LT1108, LT1109, LT1109A, LT1110, LT1111, LT1173, LTC1174, LT1300, LT1301 and LT1303.

Technical Books

1990 Linear Databook, Vol I —This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook, Vol II — This 1248 page supplement to the 1990 Linear Databook is a collection of all products introduced in 1991 and 1992. The catalog contains full data sheets for over 140 devices. The 1992 Linear Databook, Vol II is a companion to the 1990 Linear Databook, which should not be discarded. $10.00

1994 Linear Databook, Vol III —This 1826 page supplement to the 1990 and 1992 Linear Databooks is a collection of all products introduced since 1992. A total of 152 product data sheets are included with updated selection guides. The 1994 Linear Databook Vol III is a companion to the 1990 and 1992 Linear Databooks, which should not be discarded. $10.00

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